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VOLUME 3 NUMBER 4

Serial Switch Fabrics: A Qualitative and Numerical Analysis

TECHNOLOGY FEATURE:

**Concurrent hardware and
software design for devices**

APPLICATION FEATURE:

**Rich graphical interfaces for
remote embedded applications**

PRODUCT GUIDE FEATURE:

Mezzanine cards benefit TEMs

PRODUCT GUIDE:

AMCs and PrPMCs

InfiniBand

RapidFabric

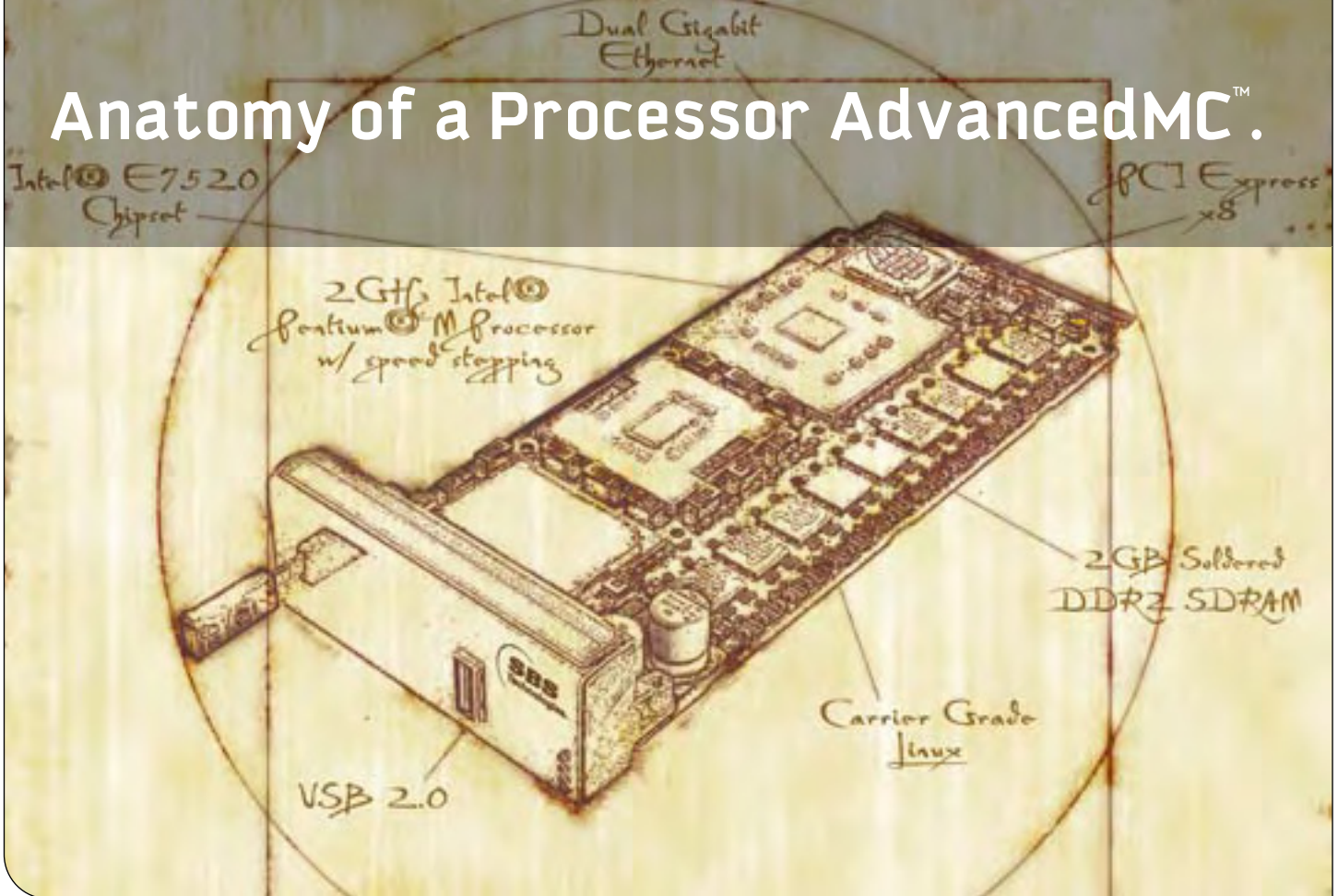
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COVER

The race is on for serial fabric product introductions and market acceptance.

PRODUCT

The KosiPM AMC module from Artesyn Communication Products features an Intel Pentium M processor, dual GbE ports, Carrier Grade Linux support, and PCI Express connectivity.

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Serial Switch Fabric Update

Welcome to the July issue of *Embedded Computing Design*. This issue includes a thorough serial switch fabric article from IDT that goes far beyond the usual textual explanation. You will want to save this one for future reference. As always, we also feature other in-depth articles on current topics for the ever-growing embedded community.



Mark David Barrera

Serial Switch Fabrics

■ *Evaluating high speed industry standard serial interconnects*, by Harpinder S. Matharu of IDT. Harpinder thoroughly describes the InfiniBand, RapidFabric, and Advanced Switching Interconnect (ASI) serial switch fabrics. He compares each of the three competing architectures by focusing on their flow control, congestion management, and high availability characteristics. This article includes a great deal of numerical information.

Concurrent Device Design

■ *Embedded device development requires concurrent hardware and software optimization*, by Rindert Schutten and Thomas Anderson of Synopsys. Rindert and Thomas point out that the traditional sequential design flow where hardware is developed before software no longer fits the needs of today's complex system designers. This article includes a nice figure that illustrates the contrasts between a sequential and concurrent design flow.

Embedded Graphical Interfaces

■ *Rich graphical interfaces for remote embedded applications*, by Nate Smith of Microchip Technology. Nate describes how you can use a Web browser to remotely control an application. The application uses a microcontroller with an installed TCP/IP stack, in conjunction with an Ethernet controller. There are significant cost benefits for an application, as it does not require the integration of an application resident graphical interface such as an LCD screen.

Mezzanines for Telecoms

■ *Standard mezzanine interfaces facilitate outsourcing for telecom OEMs*, written by Todd Wynia of Artesyn. Todd describes the evolution of mezzanine cards, and their benefits for telecom OEMs. This article includes information on PMCs, PrPMCs, and AMCs. It also describes MicroTCA shelves for AMCs. These shelves do not require AMC carrier boards. Instead, the AMCs are plugged directly into the MicroTCA shelf. I envision this as a very clean solution for many low to midrange applications.

As always, I encourage your comments and suggestions concerning this and future issues. Please do not hesitate to send in an article abstract for any complex or controversial subject.

M. D. Barrera

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Looking Forward >>>>

The ECD September issue is our annual Product Directory.

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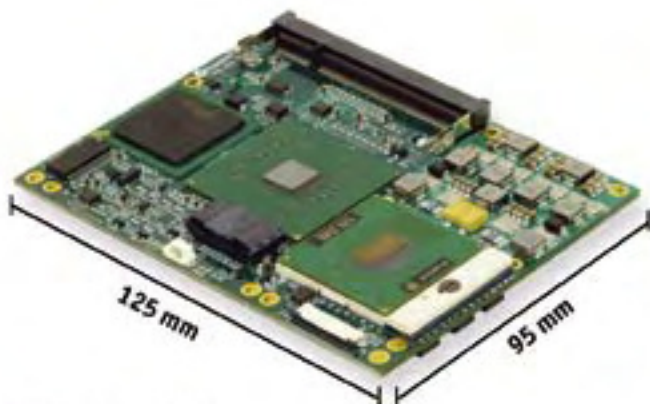
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By Don Dingee

Buy one processor, get one almost free

Multicore processors

We have now fully entered the age of the multicore processor. It has only been a short time since desktop class dual core parts have been announced, and I am already starting to feel like I have to have one in my machine just to keep up with the neighbors. But there are broader implications of this new age for all of us.

As with many computing advances, this innovation was spurred by the embedded computing industry vendors who have known the effectiveness of multicore

architectures for years. The trend toward multicore is dramatically changing the entire computing industry as higher end processors become available in dual core versions, creating new options for designers to approach problems and affecting how most vendors will offer products in the near future.

Packing them in

The prevailing thinking for the last 15 years was silicon was cheap and transistors were free, but this has undergone a sea change. We have now learned that

too many transistors in too small a space is very, very expensive. It has become prohibitive to simply continue to pack more transistors, especially power hungry memory interfaces and I/O drivers, into today's 90 nm and tomorrow's 65 nm and smaller process geometries without causing drastic power consumption and thermal problems.

Leakage and power

Leakage, once negligible in CMOS transistor integrated circuits that only consumed power during switching, is



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now a mounting problem as geometries have gotten smaller and clock speeds have increased.

According to Freescale Semiconductor, the power leakage for a 90 nm process device is two to three times more than for a 130 nm process device at the same voltage. This more than offsets the gains from geometry and core voltage reductions.

By including a second processor either on the same die or in a second die within a single package, surrounding logic such as

bus interfaces can be shared and power can be conserved as compared to a traditional dual package, dual processor solution.

Current availability

With the recent round of announcements in 2005, every major processor architecture is now offered in a homogenous, single-chip dual core (or in some cases more) solution. The following vendors now offer multicore processors:

- | | |
|------------|--------------|
| ■ AMD | ■ Cavium |
| ■ Broadcom | ■ Centrality |

- | | |
|-------------|--------------|
| ■ Freescale | ■ PMC-Sierra |
| ■ IBM | ■ Sun |
| ■ Intel | ■ TI |
| ■ NEC | ■ Via |

If FPGA cores that can be combined by designers into custom devices are considered, we can add the following vendors:

- | | |
|----------|-----------|
| ■ Altera | ■ MIPS |
| ■ AMCC | ■ Renesas |
| ■ ARM | ■ Xilinx |

Pushing the envelope

Designs with more than two cores are already showing up in the marketplace. Broadcom now has a 64-bit quad core MIPS System-on-Chip (SoC). The IBM Cell processor implements a 64-bit PowerPC core with eight additional synergistic cores, allowing up to ten simultaneous threads and over 128 outstanding memory requests (Figure 1). These new platforms are continuing to push processing density and give designers unheard of flexibility in processor architecture, and are sure to be followed with similarly exciting developments from other SoC vendors.

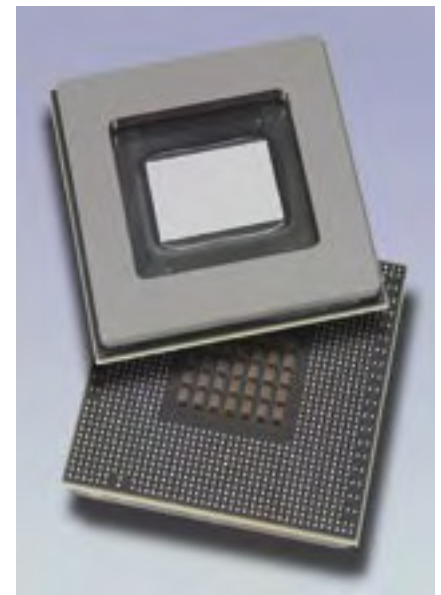


Figure 1

Multicore cost

What do multicore processors mean for system costs? Of course, embedded systems designers have to pay for the silicon and the first processor with its supporting I/O. But suddenly, the second processor is now almost free (at least for the lower clock speeds with their better yield points).

If we take this idea further, processor cores will be incrementally free going forward as multicore architectures become

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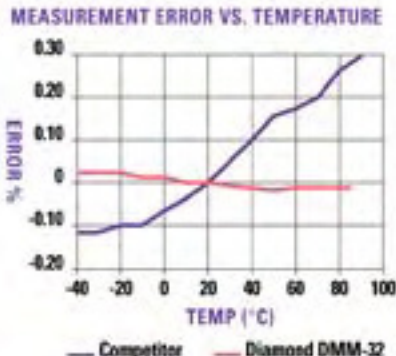
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popular. Intel is already implementing hyperthreading technology on dual core Pentiums, and has stated that for 2015 they are aiming for "tens or potentially hundreds" of processor cores per die. With at least fifteen projects underway, Intel will drive the adoption of dual core in the mainstream.

Software support

Software vendors are starting to take notice as well. In response to dual core announcements from AMD and Intel and pressure from Linux alternatives, Microsoft recognized that its pricing model needed updating and took a bold new position on multicore software pricing in October 2004.

In this excerpt from the Microsoft website dated January 2005, we see the term *single processor* redefined: "To support customers' business needs and use of new technologies, Microsoft generally considers multicore and hyperthreaded processors to be a single processor, regardless of the number of cores and/or threads that they contain."

The interesting question is if any of the royalty-based Real Time Operating System (RTOS) vendors will respond and price their products for multicore processors as if they were a single processor. The answer to that question may lie in how popular asymmetric applications become.

Microsoft seems to be making a Symmetric MultiProcessing (SMP) assumption in their pricing model, where all cores operate with the same operating system and threads are distributed as soon as a core is available.

But creative embedded system designs could take strong advantage of running different operating systems on cores, such as combining Linux and an RTOS on a dual core processor with each having their own core. Or, royalty-free RTOS platforms may become even more popular on processors with many cores. It is not hard to imagine a design where the same purpose-built optimized kernel is used on multiple cores within a multicore processor.

Throughput

Two cores probably will not have the same aggregate throughput as two separate processors in most cases, but the response time for a given thread will probably be quicker.

What happens when we get to the hundreds of cores target, and each thread has its own core? Imagine the possibilities. I can almost hear the footsteps of software designers running down the hall to their boss' office, while frantically yelling "When do I get my own core to run on?"

When additional processor cores are free (or asymptotically close to it), embedded systems designers will have very interesting options for creating new breakthroughs. I am looking forward to observing how designers reap the benefits. As always, I welcome your feedback, and would like to hear about how multicore processors affect your current and future designs. You may e-mail me at: ddingee@opensystems-publishing.com

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Eclipse plug-in survey

The real power

The real power of Eclipse lies in the availability of released plug-ins. Hundreds of plug-ins are now available to the general public even though membership in the Eclipse Foundation did not rapidly escalate until just last year.

In this column, I list the wide diversity of plug-ins that caught my eye as a former software engineer. For convenience, tabularized summaries of the open source and commercial plug-ins are included at the end of this column. Note that much of the following information is excerpted from the developer's website.

Open source plug-ins

Checkclipse

From Marco van Meegen. Checkclipse integrates the Checkstyle style checker for

Java Coding Guidelines into Eclipse. While you develop, style violations are marked in the Workbench by warning markers and task entries. Checkclipse features the following:

- Checks for code formatting
- Checks for complete javadoc tags
- Checks for very long methods and long parameter lists
- Checks for identifier naming conventions for classes, parameters, and members

Continuous Testing

From David Saff. Continuous Testing builds on the automated developer support

in Eclipse to make it even easier to keep your Java code well-tested, if you have a JUnit test suite. With continuous testing enabled, as you edit your code, Eclipse runs your tests quietly in the background, and notifies you if any of them fail or cause errors. It is most useful in situations where you would already have a test suite while you are changing code:

- when refactoring
- when performing maintenance
- when using test-first development

EclipseME

From the EclipseME development team. EclipseME is an Eclipse plug-in to help develop J2ME MIDlets. EclipseME performs the grunt work of connecting J2ME Wireless Toolkits to the Eclipse development environment, thereby allowing you to focus on developing your application rather than worrying about the special needs of J2ME development.

Fat Jar

From the Fat Jar development team. The Fat Jar plug-in is a deployment tool that deploys an Eclipse java-project into one executable jar. In addition to the eclipse standard jar-exporter, referenced classes and jars are included in the *Fat Jar*.

Google Search

From Chris Kau and Tom Pesic. This plug-in allows you to access Google from within Eclipse. Very useful when you need software tips and other information.



By Mark David Barrera

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PICdt

From Luke Hirschy. The eclipse-picdt plug-in provides an open-source, cross-platform software development environment for the entire line of Microchip PIC microcontrollers.

WebApp

From BlueSkyTime. The WebApp Plug-in is a tool designed to help with the development of web applications within Eclipse. The plug-in provides the ability to:

- Install web application servers
- Switch between installed servers
- Create blank web application projects
- Start, restart, and stop web application servers
- Launch web application projects into web browsers
- Import and export web application projects from or to Web ARchive (WAR) files
- The plug-in also provides some debug support and a framework for developing web application server adapters.

Commercial plug-ins

ClearCase

From IBM Rational. Provides a ClearCase plug-in for the Eclipse development environment. IBM Rational® ClearCase® provides life cycle management and control of software development assets. This plug-in provides Rational ClearCase functionality to Eclipse users for a tightly integrated Software Configuration Management (SCM) solution.

DataScope

From AFTI. DataScope is an extensible JDBC plugin for the Eclipse IDE that allows easy and universal access to and modification of resources within a database.

Glider

From Ensemble Systems. Glider for Eclipse provides a run-time container that lets you instantly debug your EJB application. Code, compile, and debug J2EE applications before you deploy to your application server.

IntraWeb

From Atozed Computer Software. IntraWeb utilizes a visual designer to allow

pages to be designed visually in a form like manner. The designer supports advanced features such as panels, form inheritance, aligns, and even BorderLayout. Simply drop controls on the page, set properties, create events, and run.

Java-COM Bridge

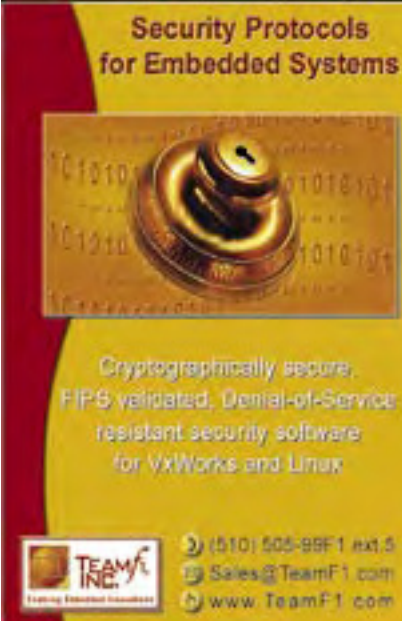
From IBM alphaWorks. Development Tool for Java-COM Bridge is a tool for developing and enabling tight communication between Java and COM-based applications. This enables the integration of both COM- and Java-based components in one application and allows the two kinds of components to communicate bi-directionally through the Java Native Interface (JNI) technology.

JFaceDbc

From Michele Puopolo. JFaceDbc is a cross platform database tool, written as an Eclipse plugin. JFaceDbc enables multiple simultaneous connections to many different databases. It has a rich database structure viewer, and a rich SQL editor with syntax highlighting and table names auto-completing. You can use the Graphical Database Visualizer to inspect relationships among tables.

Openmake

From Catalyst Systems. Openmake eliminates the need to code XML or build specific Java Classes for ANT while enabling a single build process for the enterprise. The primary goal of the Openmake plug-in is to allow developers to continue working within their IDE while enabling their organization to standardize how applications are built regardless of platform, compiler or IDE.



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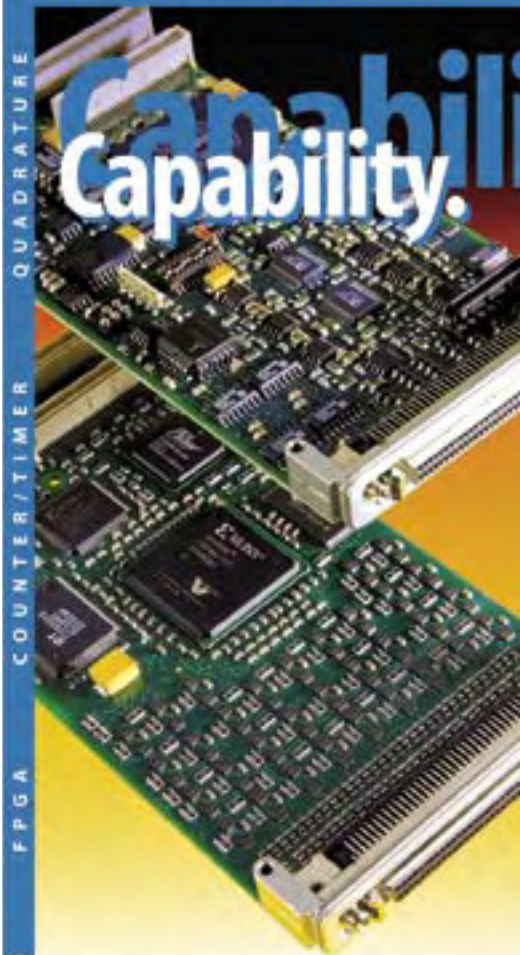
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Together Edition

From Borland Software. Together Edition for Eclipse speeds the application development lifecycle by integrating the Eclipse platform with a design-centric solution built to visually model software, measure quality, and improve team productivity. A visual bridge among end users, architects, and developers.

XMLBuddy

From Bocaloco Software. Supports XML and DTDs. Generates DTD from an XML instance. Validates and provides code assist based on DTDs or document contents (no DTD). Performs user-configurable syntax coloring. Performs optional auto-validate and auto-format (flow) while you edit. Dynamically updates outline view.

Enhanced encoding support auto-detects document encoding per the XML 1.0 specification.

XMLSpy

From Altova. XMLSpy 2005 Enterprise Edition is an XML development environment for modeling, editing, debugging, and transforming all XML technologies. XMLSpy automatically generates runtime code in multiple programming languages.

Future columns

I am open to any suggestions from the Eclipse community for future *Eclipse News* columns. You may e-mail your ideas to me at: mbarrera@opensystems-publishing.com

Web Resources

Eclipse Foundation plug-in directory:
www.eclipse.org/community

Eclipse Plugin Central (EPIC):
www.eclipseplugincentral.com

Open Source Plug-in	Website	Application
Checkclipse	www.mvmsoft.de	Uses Checkstyle to check Java source code.
Continuous Testing	pag.csail.mit.edu/continuuotesting	Eclipse runs your code tests in the background.
EclipseME	eclipseme.org	Integrates J2ME Wireless Toolkits into Eclipse.
Fat Jar	fjep.sourceforge.net	Deploys an Eclipse Java project into one executable jar.
Google Search	www.fatborn.org/eclipse/plugins/google	This plug-in allows you to access Google from within Eclipse.
PICdt	sourceforge.net/projects/eclipse-picdt	Software development environment for Microchip PIC microcontrollers.
WebApp	blueskytime.sourceforge.net	Web application development.

Table 1

Commercial Plug-in	Website	Application
ClearCase	www.ibm.com/developerworks/rational	Provides a ClearCase plug-in for the Eclipse development environment.
DataScope	aftiplugins.com/datascope	JDBC plugin for Eclipse that allows database viewing and modification.
Glider	www.ensemble-systems.com/glider	A run-time container that lets you debug your EJB application.
IntraWeb	www.atozed.com/intraWeb/Java	A visual designer to design pages visually in a form like manner.
Java-COM Bridge	www.alphaworks.ibm.com/eclipse	Enables the integration of COM- and Java-based components in an application.
JFaceDbc	www.jfacedbc.com	JFaceDbc enables multiple simultaneous connections to different databases.
Openmake	www.openmake.com/dp/eclipse	Openmake enables a single build process for the enterprise.
Together Edition	www.borland.com/together	Visually model software, measure quality, and improve team productivity.
XMLBuddy	www.xmlbuddy.com	Supports XML and DTDs and generates DTD from an XML instance.
XMLSpy	www.altova.com/features_eclipse.html	XML development environment that generates runtime code.

Table 2

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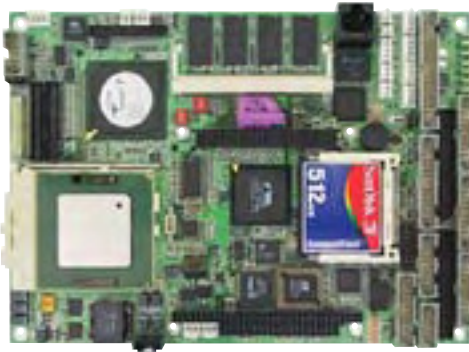


Back View

- PCI/LPC/SMB Bus
- CRT/LCD video
- Dual channel enhanced IDE
- 10/100Base-T
- AC'97 2.2 Audio
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- 1 LPT Port
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- 8 GPIO Ports
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Embedded automotive market and conferences



By Hermann Strass

Embedded automotive market

In this issue, I will discuss the embedded automotive computing/electronics market in Europe. The automotive market is one of the largest consumers of embedded electronics products in Europe.

In Germany, the embedded automotive market comprises the largest share of the embedded market (almost 43 percent), according to the central organization of the electrical and electronics industry in Germany (ZVEI).

In PCB consumption, automotive is in the number three position in Europe (22.1 percent) and growing fast (23.4 percent last year). Germany produces the most PCBs in Europe (34.8 percent), and the automotive sector is in the number one position (32 percent market share and 37.2 percent AGR). The automotive sector is also the largest consumer of connectors (37 percent) in Germany.

It is estimated that the automotive consumption of embedded electronics will increase by about 11 percent per year up to 2008 when Europe will be the biggest automotive market (about US \$10 billion), almost double the American market, and more than double the Japanese market.

Increasing automotive use

About 25 percent of the value of today's automobiles is in electronics. This is estimated to increase to about 40 percent in 2010. The real challenge is the unusually high complexity of such electronic systems and the required diversity in controller types, bus systems, and architectures under extreme environmental and longevity requirements.

European presence

European automotive semiconductor companies have a significant presence as shown below:

- Freescale (USA) is number one, with European centers of excellence in Wiesbaden and Munich.
- Infineon (GER) is number two.
- STMicroelectronics (FR/IT) is number three.

There are also highly specialized semiconductor companies, like ELMOS (GER) who sell directly to automobile manufacturers rather than to the open market. Bosch (GER) is now the world's largest supplier of electrical and electronic goods to the automotive industry.

Automotive reliability

It is true that an embedded automotive electronics failure may put the health and welfare of consumers at risk. That is why embedded automotive systems have to be orders of magnitude more reliable than normal systems under extremely adverse environmental conditions.

Just imagine what would happen if you had a *blue screen* at 240 km/h (149 mph), the maximum speed limit set by automotive electronic systems for most automobiles sold



Figure 1

in Germany. Qualification according to ISO/TS 16949 is therefore mandatory for the automotive industry.

Embedded automotive products

Automotive LifeCycle Solutions

The ETAS Group (GER), a spin-off from Bosch with worldwide subsidiaries, supplies *Automotive LifeCycle Solutions* to the automotive industry. This includes embedded electronics, test equipment, and design tools that accompany an automobile from the design stage through production and garage testing. It can also be used to simulate future embedded automotive electronics.

ETAS has established a life testing lab for automotive electronic design engineers. Dr. Bortolazzi (DaimlerChrysler, Stuttgart) of ETAS lectures on *Systems Engineering in Automotive Electronics* at the FZI (Research Center Informatics) in Karlsruhe, Germany. The lab falls under the direction of under Prof. Dr. Klaus D. Mueller-Glaser and Dipl.-Ing. Markus Kuehl.

After the embedded engineering students complete their dry course and perform simulations, they get a production model of the *smart roadster* from a subsidiary of DaimlerChrysler (Figure 1).

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First, the students use the ASCET product family of development tools and INCA application software from ETAS to simulate optimum throttle settings for lowest possible fuel consumption during a smooth ride.

Next, the standard engine control electronics are removed, and the students have to drive with engine control hardware and software that they have developed. During the drive, they optimize idling using heads-up displays and notebook computers that display many of the internal parameters. Optimization is therefore performed on the road as opposed to on a test stand.

The embedded engineering trainees soon learn that designing and optimizing an automobile engine controller is one of the most difficult and complex jobs for any embedded designer. Nothing is linear and everything is interdependent. A display of the parameter dynamics looks like a view of the Rocky Mountains with peaks and valleys in an irregular arrangement.

A few examples illustrate what an embedded design engineer has to manage. For instance in the past, as a driver depressed the accelerator pedal, more fuel was injected into the engine. At times, this resulted in an excess of fuel to the engine. Modern day embedded electronics ensure that the proper amount of fuel for the current conditions is supplied to the engine so that fuel is not wasted, and the engine will not be harmed by partially burnt fuel.

As another example, we all know a car performs better on a cool morning. Cool air is more compact, and therefore contains more oxygen per volume. The engine can burn gasoline more completely, which increases performance (immediate horsepower). This means that an embedded designer has to take into account:

- moisture
- elevation
- current rpm
- air temperature
- accelerator position

These parameters have to be processed in real time so the fuel injection, ignition, and other controls can be set for optimum performance for minimum fuel consumption and smooth engine operation. In addition, all of the embedded systems have to be designed to last for at least 10 years of trouble-free operation in an environment that can range from the heat of the Arizona desert to the cold of a Minnesota snowstorm.


Basic Telematics Unit

Infineon and Volkswagen have designed the *Basic Telematics Unit* for use in Volkswagen automobiles. In a holistic approach, VW wants to create a stable electronics system in a moving car. The basic telematics unit is based on the Infineon TriCore 32-bit chip architecture. It also uses the Infineon SingleStone module for Bluetooth applications, its GPS chip set for satellite-based positioning, and its GSM/GPRS chipsets for mobile communication and internet access.

The software architecture and the modular, reusable software package designed by Volkswagen are completely based on open standards. The Basic Telematics Unit is available to carmakers and automotive suppliers.

As a simple example of the telematics unit capabilities, consider the problem of the often legally required hands-free operation of a mobile phone in a car. The unit would get the data from any passenger's Subscriber Identification Module (SIM) card from their mobile phones and

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Figure 2

automatically divert calls to the unit. Short Message Service (SMS) messages, telephone numbers, or names of callers will appear on the instrument panel display. The driver can dial telephone numbers by voice input or by using controls on the steering wheel. In case of an accident, automatic calls can be sent to the nearest repair shop and to a chosen recovery service.

Ultra plush office on wheels

Maybach is the name of the most luxurious car model from DaimlerChrysler in Germany. Wilhelm Maybach was the chief car and engine designer of Daimler-Benz in the late 1800s. In 1901, he introduced the first Mercedes.

Passengers of the Maybach Brabus SV 12 Biturbo (Figure 2) can surf on the internet or listen to Dolby Surround Sound and watch movies on two 15.2 inch screens while traveling at speeds up to 314 km/h (195 mph). In this automobile, the top speed is not electronically limited to 240 km/h (149 mph) like most European models.

The 12 cylinder biturbo engine produces 471 kW (640 metric hp) and accelerates from zero to 100 km/h (60 mph) in 4.9 sec. As the experts know, it is not easy to sustain continuous wireless reception and transmission at such high speeds. The Universal Mobile Telephone System (UMTS) protocol is used for wireless communications for this automobile.

Embedded automotive conferences

Munich, Germany hosted the DATE conference (Design, Automation and Test in Europe) from March 7-11. Sponsors

include the IEEE Computer Society and the EDA Consortium.

The event held a Special Automotive Day on March 9. Dr. Bortolazzi of DaimlerChrysler (mentioned previously) moderated an automotive keynote about AUTomotive Open System ARchitecture (AUTOSAR) by Mr. Harald Heinecke from BMW. He also moderated tracks on automotive computing design platforms and on automotive architectures.

An automotive designer's forum (Kfz-Elektronik) will be held on May 11 in Ludwigsburg/Stuttgart, Germany with tracks on:

- Hardware
- Multimedia
- Test and debugging
- System design and quality
- FlexRay interconnect protocol
- Software quality and security

National Instruments Germany (Munich) will hold a one-day technology conference about testing, modeling, simulation, and data management in the automotive industry on June 7, 2005 in Wolfsburg, Germany at the doorsteps of the world headquarters of Volkswagen.

Hermann Strass is an analyst and consultant for new technologies, including industrial automation, computer bus architectures, mass storage technologies, and industrial networking. He is the author of several books and trade magazine articles, and an active member of several international standardization committees.

To learn more, e-mail Hermann at: hstrass@opensystems-publishing.com

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By Bill Weinberg

Closing gaps in the embedded Linux ecosystem: The ISV challenge – Part I

In this column, Bill examines the state of the embedded Linux ecosystem – how Independent Software Vendors (ISVs) regard Linux as a platform, how they port to Linux, and how they offer support for the ever-expanding range of Linux distributions and processing platforms.

Part I of the column examines factors that can slow or limit ISV adoption of Linux as a host/target. In Part II, the column details efforts by the OSDL and other organizations to facilitate and accelerate ISV adoption and support of Linux.

Inherited benefits

Embedded computing with Linux benefits enormously from the mainstream adoption of Linux and open source for the enterprise. Embedded developers today leverage Linux to build intelligent devices ranging from telecommunications to home networking, from industrial control to medical instrumentation, and from home entertainment to smart phones. However, embedded development and deployment with Linux also face many of the same challenges as enterprise applications. Standing out among those hurdles is the validation and productization of Commercial Off-The-Shelf (COTS) software from ISVs on Linux platforms.

The ISV challenge

In the enterprise marketplace, ISVs view Linux as an emerging and increasingly dominant host platform for data center and desktop applications.

Most visibly, Linux has been taking server and workstation market share away from

proprietary UNIX, as well as winning white boxes, blades, and seats away from Microsoft Windows. The first ISVs to migrate their wares to Linux have been those with off-the-shelf UNIX product lines.

Enterprise and embedded ISVs choose if and when to support Linux based on a mix of ROI factors. To understand these factors, the OSDL conducted a study in 2004 of several dozen top-tier (enterprise) ISVs. The highlights of the study are shown in Table 1.

The study data bears some additional analysis. The number of distributions supported by an ISV seems innocuous out of context, but bear in mind that these same companies typically support only one or two versions of Windows or Solaris. The extreme of nine distributions is for ISVs in the storage area market, whose middleware and appliances must support regional distributions of Linux (such as Red Hat, SuSE, Mandriva, and Red Flag) and legacy distributions of Linux of the same for the lifetime of their appliance.

Study Highlight	Finding
Average number of distributions supported per ISV	3.3
Number of ISVs targeting two or more Linux distributions	84%
Most distributions/versions supported by one ISV	9

Table 1

Surprisingly, many enterprise software vendors do not track actual deployment or sales by host OS, and consequently, they do not respond directly to movement in their existing customer base. A more common migration motivator is requests from new customers, or pending orders from large accounts.

The OSDL study also revealed the following pervasive set of concerns shared by most ISVs:

- Validation and testing of ISV-ware with each release of leading Linux distributions
- Library version differences among distributions
- Identifying distributions and versions to support
- Packaging for and installation on multiple distributions

Certainly, these concerns are shared by software houses targeting embedded as well. Following is a discussion on how these issues have the most impact on ISV ROI.

Port once and run everywhere?

While the Linux kernel is impressively stable and community practices prevent the OS core from forking or fragmenting, it is very difficult to guarantee that an application binary built on one Linux distribution will run correctly on another – even within the family of IA/x86 distributions. While the divergences are small, and many programs simply do *just run* on one distribution or another, for

complex applications these differences can be enough to derail successful installation and execution. Problem areas are listed in Table 2.

In enterprise, companies like Red Hat, SuSE, Mandriva, and others address these challenges with a combination of platform certification programs and language in their Service Level Agreements (SLAs) that determines support policies for third-party commercial and open source programs not included in their own distributions. More encompassing efforts to address these issues have also included United Linux (now defunct) and the Linux Core Consortium.

Additional challenges

Independent software vendors who offer embedded applications face the above challenges in varying degrees, as well as additional challenges endemic to embedded development and deployment. For nominally embedded applications running on enterprise-like blades and embedded PCs, the challenges are mostly the same. With other more deeply embedded designs, other unique obstacles present themselves:

- While there are probably fewer embedded ISVs overall, those ISVs may need to address a greater number of divergent platforms and application areas.
- While all architectures share the same Linux kernel source base and most other operating system code, there are differences in maturity and feature support among CPU-type implementations.

Problem Area	Example
Included run-time library versions	glibc, xlib
Included key tool and utility versions	gcc, perl/PHP
Included installed package versions and interdependencies	Distributions typically have hundreds of packages.
Desktop choice	Gnome, KDE
Frameworks	GTK, QT, QT/e
Underlying Linux kernel version	2.4 versus 2.6
Loadable module (driver and kernel extension) dependencies on kernel versions	2.6.8 versus 2.6.10
Differences in packaging and installation paradigms	Red Hat versus Debian

Table 2



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- There exist a larger number of relevant commercial embedded distributions and platforms than exist for enterprise Linux (each with smaller market shares and volumes), and there are more differences among those products (FSMLabs, MetroWerks, MontaVista, TimeSys, SysGo, Wind River).
- While there exists the possibility of binary compatibility across x86/IA-32 enterprise distributions, there is no comparable potential across the major embedded architectures (such as ARM, M68K, MIPS, PowerPC, SH, x86). Indeed, there are even source and binary validation issues among members of the same CPU family (such as Intel XScale vs. TI OMAP, IBM vs. Freescale PowerPCs).
- Many embedded ISVs do not actually target Linux per se, but port to Linux using compatibility layers. On one hand, these abstractions minimize differences among embedded operating systems, but on the other hand, they mask and do not address importance distinctions between them (for example, threading library semantics).
- In harmony with open source practices, many embedded ISVs have long-standing traditions of shipping source code. However, this supply method shifts the burden of embedded platform validation and support to their customers (and creates services opportunities for themselves or third parties).
- Much ISV-ware was conceived to bridge the gap between enterprise and infrastructure technology and *bare metal* embedded applications. Much of this value added software addressed management middleware, file systems, and networking protocols – technology that is fully native to all embedded Linux platforms. To play in the embedded Linux market, embedded ISVs must decompose their offerings to face this reality, or force-fit their legacy wares onto the embedded Linux OS and stack, with questionable value-add for customers.

It is also interesting to examine how embedded software companies *dip their toes* into supporting Linux. Typically, embedded ISVs start by targeting their wares at the regionally-dominant enterprise Linux platform. In North America, this first port is usually to a version of Red Hat. Many ISVs go no further than this first platform-wise step, and then proceed to advertise they have accomplished Linux support.

More systematic Linux support by embedded ISVs usually involves validation on one or more architecture versions of a

particular embedded Linux distribution, such as MontaVista Linux Carrier Grade Edition, or Wind River Platform for Networking Equipment, Linux Edition.

Release introductions

In both enterprise and embedded settings, ISVs face a challenge that arises from the misalignment of their own release cycles and those of the open source platforms to which they port their wares. Most ISVs productize their applications on one or two strategic host platforms, and then port to the other OSes in their stable. Increasingly, at least one Linux distribution is usually among these key platforms.

Most ISVs of my acquaintance release new product versions every 12 to 24 months. Enterprise distribution suppliers like Red Hat and SuSE, and non-commercial distributions like Debian offer new releases as often as twice every year. Embedded platform new releases are usually introduced less often. The individual projects, whose code comprises the hundreds of packages that round out a distribution, has its own release cycle that ranges from monthly drops to more stately (or stagnant) rhythms.

"In both enterprise and embedded settings, ISVs face a challenge that arises from the misalignment of their own release cycles and those of the open source platforms to which they port their wares."

ISVs usually port their software to the current release of a given host platform, such as SuSE Desktop 9.2 or MontaVista Linux 3.1. The porting effort can occur early or later on in the platform release lifetime.

A distribution itself can draw upon hundreds, sometimes even thousands of individual project/packages. Distributions, as they approach their own code freeze dates, settle on the more recent, stable versions of their constituent package sets. Some of these packages versions might be only one month old, while others could date back 6 to 12 months.



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Misalignment

The *big challenge* occurs when an ISV, either at porting time or during the lifetime of their own release, finds a bug in a package within a distribution. The first recourse of most ISVs is to go to the distribution for a patch. The distribution supplier response,

however, may be that the bug is fixed in the next release, even if the ISV needs the patch *in the present release*.

Should the requirement escalate in urgency, the ISV may elect to go to the project behind the package (for example, GNU

binutils, qt). What they often find there is that the bug has been fixed in a subsequent release, or that the project maintainers are willing to accept or even create a patch, but on the *current release*, not on the release that was aggregated into the distribution. This mismatch is illustrated in Figure 1.

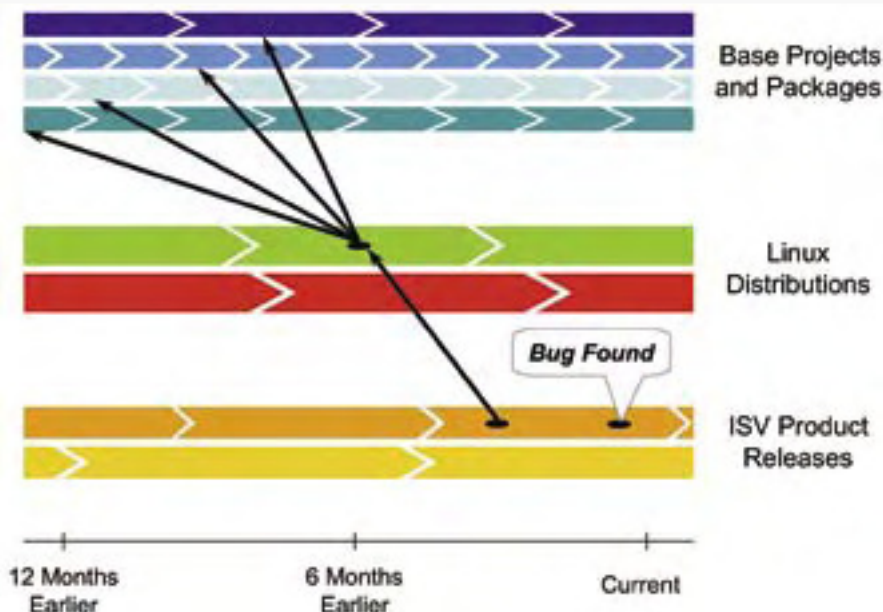


Figure 1

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In the worst case, an ISV can be faced with package code that is 12 months old. The situation for embedded ISVs can be even more precarious, since embedded Linux platform providers are often more conservative (or less agile) than their enterprise counterparts.

A prime example comes from some embedded distribution suppliers, who as of this writing still ship platforms derived from the prior 2.4 Linux kernel, a full 18 months after other distributions (embedded and enterprise) have moved to the 2.6 kernel, and most projects only build and validate their code against the 2.6 base.

Meeting the ISV challenge

In the November issue of *Embedded Computing Design*, Part II of the OSDL column will examine community and commercial efforts to make it easier for ISVs, developers, and end users in the enterprise and embedded communities. These activities and initiatives include:

- The Linux Standards Base from the Free Standards Group
- OSDL ISV and IHV Forums
- The Binary Regression Test project sponsored by the OSDL
- The Linux Core Consortium
- Partnering and validation programs at commercial distribution suppliers **ECD**

Bill Weinberg brings more than 18 years embedded and open systems experience to his role as Open Source Architecture Specialist at the Open Source Development Labs. Bill can be contacted at bweinberg@osdl.org.

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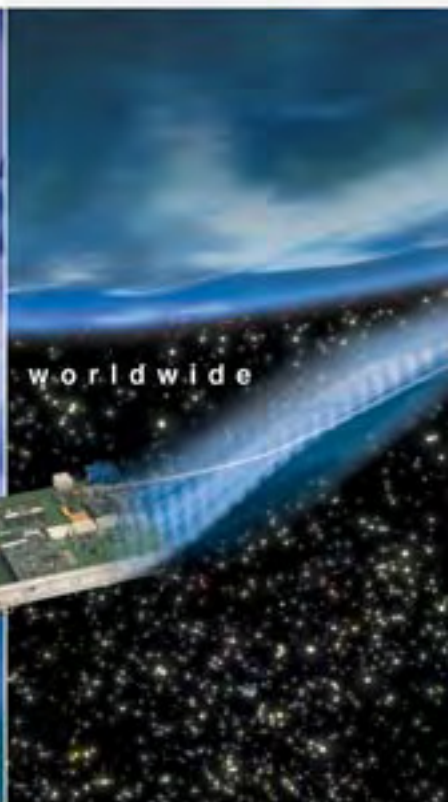
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Analog and Digital Circuits for Electronic Control System Applications

By Jerry Luecke

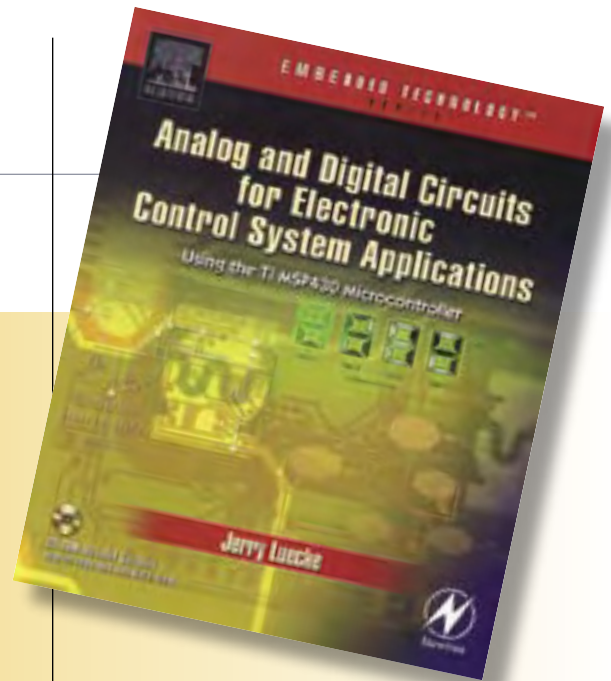
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Reviewed by Chad Lumsden

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Microcontrollers

In the vast sea of today's available electronic components, engineers have a plethora of components to choose from when it comes to embedded design. Devices such as FPGAs, DSPs, and MicroController Units (MCUs) have been in use in some form for more than 30 years. Nearly every electronic device you ever lay your hands on implements these technologies. The MCU has proven itself as one of the most reliable and effective technologies and is used in multitudes of design applications.

An extensive reference

Analog and Digital Circuits for Electronic Control System Applications has the characteristics of many of the books that are published by Elsevier as it is full of technical information and formatted in a methodical and informative manner.

The first thing that was evident when initially flipping through the pages was all the different diagrams, figures, examples, and schematics that fill the pages of this book. For nearly every idea that is covered, there is some sort of working illustration to help the reader fully grasp each concept.

The chapters are set up in a progressive manner, with each one building on the information presented in the last. Each chapter ends with a summary and a quiz, which helps enable the use of this book in a college classroom setting.

Book flow

This book first focuses on the design of the analog and digital

circuits that are used for control system applications, and then concludes with design particulars for the TI MSP430 mixed signal MCU.

The following design path for an analog control system is outlined within the chapters of the book:

- Sense the analog signals and convert them to electrical signals
- Condition the signal so it may be processed accurately
- Convert the analog signal to digital with high-speed, high-accuracy IC digital processors
- Convert the digital signal back to analog
- Output the analog signal to execute the task

Chapters 1-3

The first three chapters focus on signal paths from analog to digital, signal paths from digital to analog, and sensors.

Chapters 1 and 2 (the chapters detailing both digital and analog signal paths) offer an introduction, a refresher section, comparisons between digital and analog signals, the basics of DACs and ADCs, filtering, and conditioning and transducing of a signal.

Chapter 3 discusses temperature, magnetoresistor, light, and other sensors as well as how to implement them. Also, aspects such as angular and linear positioning, rotation, and pressure are all covered in relation to sensors within practical applications. All three chapters are scattered with extremely descriptive and helpful examples and visual aides.

Chapters 4-6

In the next two chapters, the topics switch to signal conditioning, analog-to-digital and digital-to-analog conversions, and digital system processing.

Chapter 4 covers topics such as amplification, frequency response, coupling, FET and JFET amps, op-amps, filters, and overall signal conditioning techniques.

Chapter 5 is an overview of the aspects of signal conversion. ADCs and DACs are covered in detail, with more advanced techniques explained such as high-speed conversions, and sample and hold techniques.

Chapter 6 focuses on the processing of the actual digital signal including the calculation and manipulation of digital signals. The different components of the Central Processing Unit (CPU) are explained, as well as a detailed description of actual bit manipulation within the CPU.

Chapters 7-10

The last three chapters detail assembly language programming, data communication, system power and control, and a working application created using an MCU.

Chapter 7 is an extensive overview of assembly language programming. Many of the different operations and instructions are explained, and it is full of working examples.



Chapter 8 focuses on the data transmission system with coverage of different types of data transmission protocols, and all are explained in great detail.

Chapter 9 describes system power and control with topics such as voltage regulation and dissipation, power distribution, and power supervision as some of the more detailed subjects.

Chapter 10 is a working example of a microcontroller application project from start to finish. It basically takes all the topics covered previously in the book and applies them to a real-life working application. A very nice conclusion.

Appendices

The last 100 pages are dedicated to the appendices, along with pages of reference material including the instruction set of the TI MSP430 MCU. The book also includes a CD-ROM that contains a user's guide for the TI MSP430, as well as an eBook version of the book. The detailed figures and examples coupled with the wealth of technical knowledge in this book make it a great companion for design engineers, engineering students, or anyone with a general interest in control systems and their practical application.

Jerry Luecke has almost 50 years experience in the design of semiconductor discrete-components and integrated circuits, 32 of which were spent at Texas Instruments. He has spent the last 25 years writing, editing, and publishing books about the fundamental concepts of electricity and electronics, integrated circuits, and digital electronics. He holds Bachelor and Master degrees in electrical engineering.

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Evaluating high speed industry standard serial interconnects

By Harpinder S. Matharu

Decision criteria

What performance capabilities should an industry standard switching fabric interconnect offer? Ideally, such technology should support bandwidth that exceeds the aggregate of all line cards in the system including protocol overhead, and should be capable of transporting control and data information across all the diverse entities constituting the system. In addition, latency and jitter should be minimal.

The desire for higher interconnect speeds between chips, boards, and chassis continues to grow in order to satisfy the requirement for higher throughput in future systems. It is now apparent that parallel shared-bus architectures no longer provide a viable option.

To address these requirements and challenges, some communication equipment manufacturers have turned to proprietary high-speed interconnects. However, these are short term solutions due to their high cost, long-lead time, and lack of interoperability between proprietary interconnects.

Over the long term, equipment designers need industry-standard solutions capable of sustaining high speed data transfer at low cost. Based on earlier communication standards, new serial interconnect technologies such as InfiniBand, RapidFabric, and Advanced Switching Interconnect (ASI) deliver an industry-standard approach. This approach allows equipment designers to reuse software and maintain backward compatibility with legacy equipment while leveraging the cost efficiencies of the existing infrastructure.

In this article, Harpinder first describes each of the three architectures. He then compares each of these three competing architectures by focusing on their flow control, congestion management, and high availability characteristics.

An interconnect fabric must also provide flow control capabilities to ensure a high Quality of Service (QoS) level. To achieve this goal, the system must provide congestion management policies and mechanisms capable of preventing an overload of the link and component capacities within the fabric. In addition, the fabric must provide the right balance of capabilities to support diverse applications without driving up device complexity and cost.

The switch fabric should also be protocol agnostic so as to deliver a high degree of flexibility for the backplane interconnect. Its underlying topology should be designed with redundancy and failover mechanisms that support the high availability, serviceability, and reliability requirements of communications equipment.

Finally, scalability, flexibility, and extensibility are also key features in any high speed serial interconnect architecture. Ideally, the hardware should support these features and simplify deployment of fabric management software. The software should be user friendly, inexpensive, portable, extensible, and should allow centralized or distributed fabric management to support load balancing and system redundancy.

can be as simple as an Ethernet adapter or as complex as a high performance computing blade. The specification defines the hardware protocol for reliable message transport but does not define the content of the message. Hardware protocols allow data transfer from both the kernel and user spaces of the operating system.

The architecture supports a variety of fabric services ranging from configuration and asset management and error reporting to performance metric collection and topology management. It natively uses IPv6 headers to more efficiently exchange data between the InfiniBand architecture fabrics and the Internet.

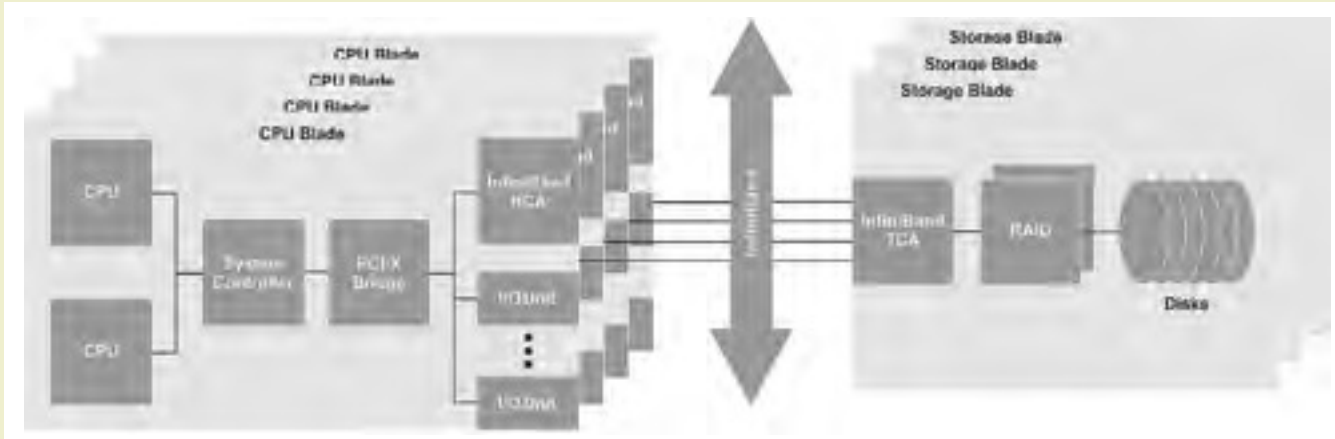


Figure 1

Architectural overviews

InfiniBand architecture

The oldest of the three discussed technologies, the InfiniBand Architecture (IBA) is a comprehensive serial interconnect specification. It was designed from the ground up to be optimized for storage area networking, high end computer clustering, and local area networking applications that require high availability and reliability. An InfiniBand server blade cluster with storage system is shown in Figure 1.

InfiniBand architecture has the following characteristics:

- Has a clock speed of 2.5 Gbps
- Supports x1, x4, and x12 lanes
- Supports throughputs of 2, 8, and 24 Gbps
- Supports module-to-module interconnects
- Supports chassis-to-chassis interconnects
- Supports QoS with 16 levels of virtual channels that are mapped to 16 service levels

InfiniBand is implemented with a four-layer stack with the following layers:

- Link
- Network
- Transport
- Physical

Devices in the system are identified by local, global, and EUI-64 addresses. Transport services provide both reliable and unreliable data delivery. Payload size can range up to 4096 bytes with up to 126 bytes of header overhead.

The architecture provides a reliable transport mechanism using messages between end nodes. Nodes in an InfiniBand configuration

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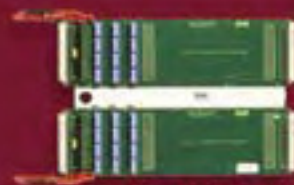
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RapidFabric architecture

Over the last two years, the RapidIO Trade Association has worked to extend the Serial RapidIO (SRIO) interconnect to cover data plane applications for telecommunications networks. The original SRIO specification supplies a simple chip-to-chip serial interconnect for processor interconnect applications and is widely used today in DSP arrays.

Designed to replace proprietary data fabrics with an open standards technology, RapidFabric adds multicast, flow control, and data streaming features to the base SRIO specification. A RapidFabric system is shown in Figure 2.

RapidFabric architecture has the following characteristics:

- Has a clock speed of 3.125 Gbps
- Supports x1 and x4 lanes
- Supports throughputs of 1.25, 2.5, and 3.125 Gbps
- Supports a bandwidth of 10 Gbps with x4 lanes

RapidFabric is implemented with a three-layer stack with the following layers:

- Logical
- Transport
- Physical

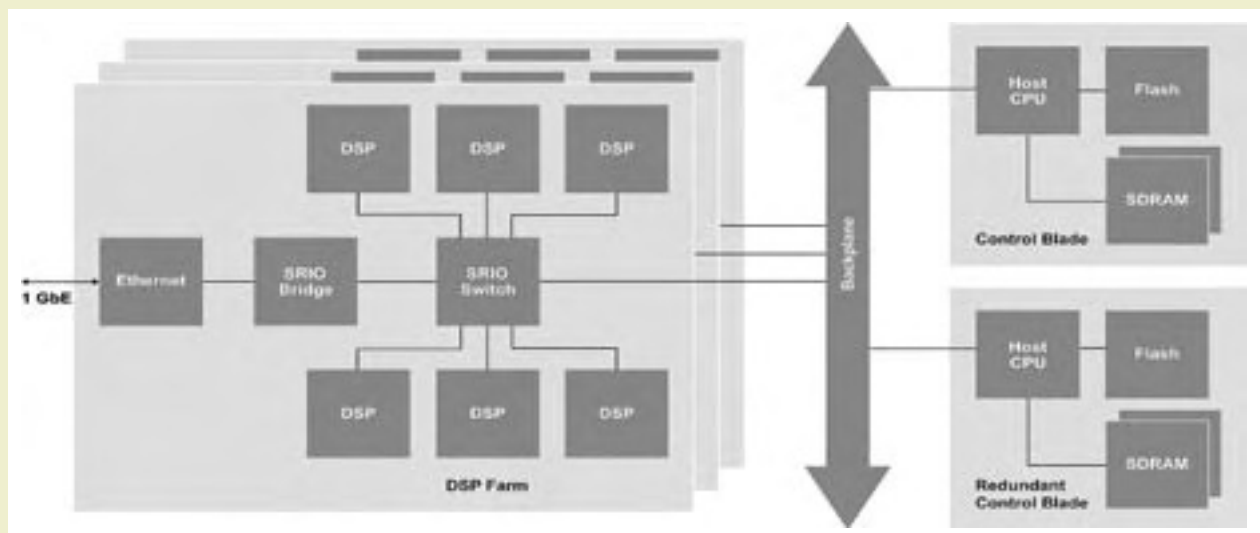


Figure 2

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The logical layer defines the protocols utilized by the endpoints to carry out interconnect services. The transport layer defines the addressing scheme for delivery. Broadcasting and multicasting capabilities are implemented by manipulating the transport information. The physical layer defines the packet transport mechanism, flow control, and electrical characteristics. It supports up to three transport flows and four virtual channels.

Devices in a RapidFabric configuration are connected by device-based routing. The architecture supports the interconnection of up to 64K devices with centrally managed routing tables. Packet headers are small. Payload size is limited to 256 bytes, but raw data streaming allows transfer of up to 64 kilobytes.

ASI architecture

Leveraging the industry's extensive investment in PCI Express (also denoted as PCIe) equipment, the ASI architecture offers developers a foundation for implementing multipoint, peer-to-peer switched interconnect links for both data plane and control plane communications. An ASI system is shown in Figure 3.

ASI architecture has the following characteristics:

- Has a clock speed of 2.5 Gbps
- Supports x1, x2, x4, x8, x12, x16, and x32 lanes
- Supports throughputs up to 64 Gbps

ASI is implemented with a three-layer stack with the following layers:

- Data Link
- Transaction
- Physical

Both the physical and data link layers replicate those used in PCIe with minor enhancements. However, the transaction layer in ASI has been completely rewritten to support the needs of a backplane interconnect.

Maximum packet size is 2176 bytes, but the architecture can support unlimited size packets through the use of a native Segmentation

And Reassembly (SAR) capability. It features path-based routing and a reliable transport mechanism with an option for unreliable delivery. The ASI packet encapsulation scheme offers low header overhead and tunnels any protocol. It provides deterministic behavior through low latency and good jitter control.

The ASI architecture provides twenty virtual channels divided into three types:

- Eight bypass capable channels are used to transport load-store protocols by incorporating mechanisms to prevent potential deadlocks
- Eight ordered-only channels are used for message oriented push data traffic
- Four multicast virtual channels are used to host any application profile

At the logical level, the standard supports eight traffic classes per virtual channel type for QoS and traffic differentiation. Primitives defined in the specification support high availability capabilities such as hot insertion/removal, redundant paths, multiple owner entities, and efficient fabric management failover.

ASI implements 127 Protocol Interfaces (PIs) for tunneling protocols and fabric management. The standard defines protocol interfaces for:

- Simple Queue (SQ)
- Simple Load Store (SLS)
- PCI Express bridging (PI-8)
- Sockets Data Transfer (SDT)

In a typical ASI fabric topology, an I/O device or CPU can natively support an ASI interface or connect to the ASI fabric using an ASI bridging device. This allows the PCIe tree hierarchy to span multiple CPU domains by using host switches and I/O switches. The host switch allows CPUs to connect to diverse I/O devices made available in the fabric through I/O switches.

CPUs can exchange data using SQ, SLS, and SDT protocol interfaces without the need to traverse the higher layer protocol stack

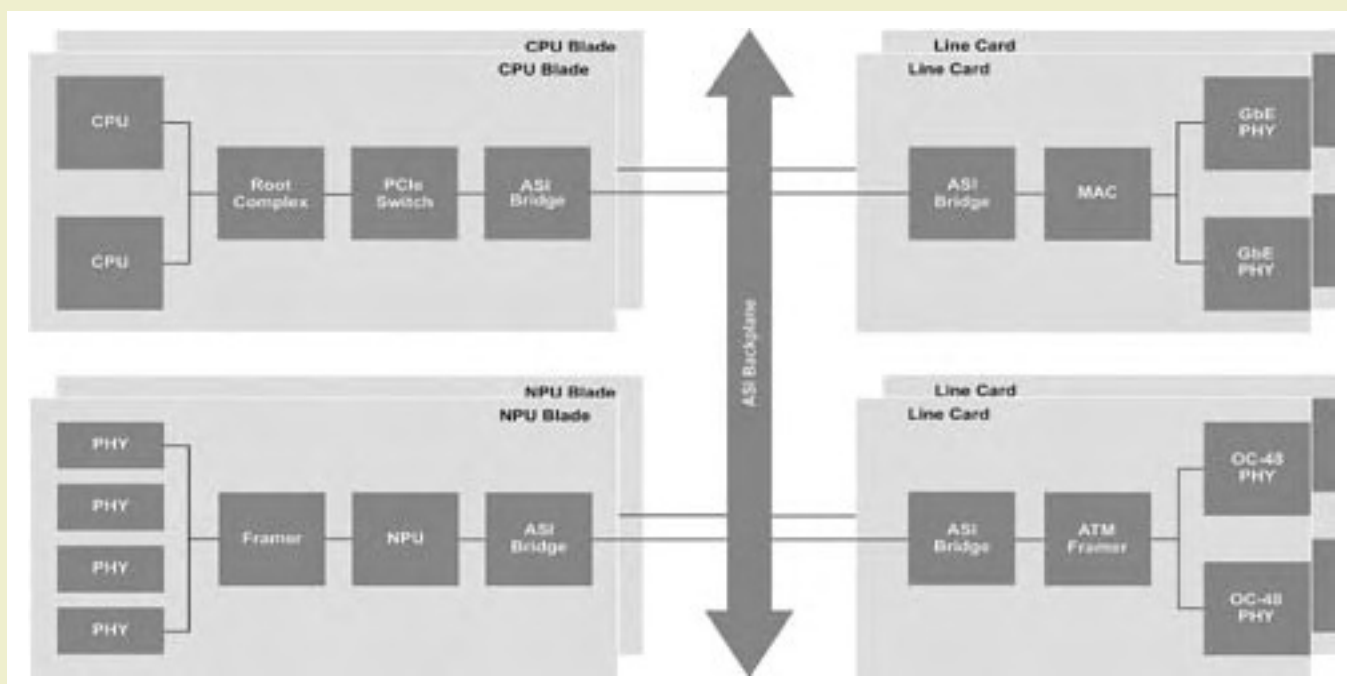


Figure 3

(such as TCP). This also allows data traffic received from an ingress NPU card to be bridged to the ASI fabric using a PI-SPI protocol interface and eventually routed to an egress NPU card.

Flow control

InfiniBand flow control

Flow control capabilities play a crucial role in each standard's ability to deliver a high QoS level. With the InfiniBand architecture, flow control is built around a credit-based scheme. When the transmitter channel adapter operates at a higher link speed than the destination ingress link speed, the intermediate switch provides *back pressure* to the transmitting channel adapter by reducing the link-level flow control credits. This function prevents the system from overrunning the resources of the slower destination device.

InfiniBand uses Virtual Lanes (VLs) to implement logical flows over a single physical link. Each IBA device supports up to 16 VLs. VL 15 and VL 0 are implemented in all devices. VL 15 is used for subnet management, while VL 0 is provided for application use. Internal device buffers are allocated separately for each VL. Each device maps a Service Level (SL) to a VL. Packets are ordered for the same source and destination Local Identifiers (LIDs) or address and SL. The system does not provide any bypass capability.

VL arbitration per port assigns the highest priority to VL 15 and the second highest priority to flow control packets. A two-level scheduling mechanism is used for all other VLs. A pre-emptive scheduler overlaid on top of a weighted fair scheme ensures fairness while allowing progress on lower priority VLs. The weighting priority and minimum forward progress bandwidth is programmable. An arbiter uses *Limit of High Priority* to indicate the number of high-priority packets that the system can transfer before a lower priority packet can be transmitted. The flow control packets send credit information to the transmitter per VL at a periodic rate.

RapidFabric flow control

In comparison to InfiniBand, RapidFabric implements a much simpler flow control mechanism. The physical layer in RapidFabric implements a 2-bit field in each packet that is used to assign priority. The logical layer defines any of three types of transaction requests (highest, medium, or lowest) that are mapped to one of the priorities at the physical layer.

Flow control in this scheme can be controlled by the receiver or the transmitter. When the receiver controls the flow, it keeps accepting ingress data on a packet-by-packet basis depending on buffer availability. If buffer space is not available, it drops the received packets and informs the transmitter by sending a packet-retry control symbol. The transmitter then waits

"The physical layer in RapidFabric implements a 2-bit field in each packet that is used to assign priority. The logical layer defines any of three types of transaction requests ... that are mapped to one of the priorities at the physical layer."

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or retransmits the packet. The receiving fabric generates flow control packets to start (XON) and stop (XOFF) the flow of traffic to it from a specific source fabric element.

When data flow is controlled by the transmitter, the system relies on a credit-based scheme. In this case, the receiver informs the source periodically how much buffer space is available and the transmitter regulates data flow accordingly.

ASI flow control

By contrast, the ASI architecture uses a credit-based flow control mechanism between peer entities per each virtual channel. A source fabric element in ASI can transmit a packet to its peer only when enough credits are available.

The ASI architecture provides twenty virtual channels divided into three types:

- Eight virtual channels are unicast, Bypass-capable Virtual Channels (BVCs) channels designed for the transport of load-store protocols. These channels can carry ordered as well as by-passable data traffic. Separate credits are allocated for the two traffic types to regulate their flow through the fabric.
- Eight channels are unicast only.
- Four channels support multicast operation.

Data traffic is differentiated and isolated through the use of different class identifiers, a virtual channel queuing mechanism, and egress link scheduling.

Peer entities determine the number of unicast BVC and Ordered-only Virtual Channels (OVCs) that each supports as part of the initial exchange of virtual channel flow control credit information. If one link partner supports more BVCs than the other, then the specification allows transformation of excess BVCs into OVCs.

ASI was also designed to support cut-through traffic. This capability allows a switch to forward a packet before it is completely received. In order to comply with credit-based flow control, the ASI route header adds credit required information for each packet. The switch reads the *credits required* field of the received packet to determine whether it has enough credits to forward it before completely receiving the entire packet.

Congestion management

InfiniBand congestion management

The InfiniBand architecture uses a static rate control mechanism to reduce the data rate sourcing speed of an end node into the fabric. Static rate algorithms control the programmable interpacket delay between packets emerging from an end point and going to the same destination.

This preconfigured value is determined by the device provided port-rate information, or by using a fabric manager-based database of best possible rates for a source destination pair. Congestion management in InfiniBand does not support any dynamic rate control schemes to allow high speed data bursts.

RapidFabric congestion management

Congestion management in RapidFabric is based on simple XON/XOFF controls on transaction request flows. Fabric elements track their internal packet buffer levels on a packet-by-packet basis that corresponds to a programmable and locally defined watermark level. If a packet-buffer level exceeds the watermark level, the receiver sends an XOFF control message to shut off the source.

Watermark levels are determined by a number of factors including a fabric element's location in the fabric, its distance from the source, and the fabric topology. They should allow enough buffer space in the fabric element for storing packets-in-flight while taking into account the worst-case XOFF latencies. When a low watermark is passed, the receiver sends an XON packet to the source to resume transmission.

ASI congestion management

ASI offers more comprehensive congestion management functions than the other two serial interface architectures. To avoid traffic congestion based on virtual channels, ASI adds three additional mechanisms:

- Status-Based Flow Control (SBFC)
- a minimum bandwidth scheduler
- end-point source or injection-rate limiting

Under SBFC, a node in the system passes status Data Layer Link Packets (DLLP) that contain information about the buffer space available at the switch to its upstream neighbor. Depending upon the status of available buffer space in the path to destination, the upstream device egress scheduler starts or temporarily suspends any flow identified by the status DLLP.

This proactive mechanism allows the system to avoid any situation where the devices run out of credits to transmit. The minimum bandwidth or vendor-defined egress scheduler can be used by devices to throttle traffic in accordance with indicated Traffic Class/Virtual Channel (TC/VC) mappings.

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ASI also supports optional source rate limiting by sorting packets into connection queues based upon criteria such as traffic class or packet path. A token bucket can be paired with each connection queue to provide source rate limiting. Token buckets provide an admission control limit to the average transmission rate per connection queue while allowing transmission of controlled bursts through the fabric. If congestion still occurs in the fabric despite these controls, it is important to quickly throttle the congesting source end point. The source can be identified by the route header.

"If a packet is received with a bad CRC or format error, then the receiver informs the sender of the error and enters an *Input Error-stopped* condition and silently discards all new packets until it receives a *restart-from-error* message from the sender."

High availability

High availability is a crucial consideration for any communications fabric. Interconnect error detection and error handling capabilities play a key role in a system's ability to implement highly efficient failover solutions.

InfiniBand availability

InfiniBand, initially designed with clustering and storage area networking in mind, offers good capabilities in this area. The error detection and handling mechanism differs at the requester and the responder. All error events are handled either at the requester or responder or at both locations.

At the requester, events can be either local or remote. Both types of errors are entered into the completion queues, which in turn invoke an event handler.

At the responder, the device can silently discard a packet, send back the error in the acknowledge packet, queue the error in the completion queue, or use a combination of all three options. A subnet manager periodically scans the fabric for changes. Alternately, the event handler can update the subnet manager.

RapidFabric availability

RapidFabric relies heavily on capabilities embedded in the RapidIO specification. To improve performance while keeping the design simple, RapidIO avoids regenerating the Cyclic Redundancy Check (CRC) as the packet moves through the fabric. However, the CRC check is performed at every hop.

If a packet is received with a bad CRC or format error, then the receiver informs the sender of the error and enters an *Input Error-stopped* condition and silently discards all new packets until it receives a *restart-from-error* message from the sender. Link maintenance control symbols are used to coordinate with the sender.

The system uses response time-out counters to detect packet loss. The port response time-out is programmable. Port error and Command and Status Registers (CSRs) indicate error conditions, which need to be reset by the software error handler.

ASI availability

ASI devotes a specific Protocol Interface (PI-5) for event handling and management. An event in ASI can be handled locally or returned to the sender. The specification also allows routing of events to a dedicated event manager.

ASI uses the link layer, transaction layer header, and payload CRCs to perform packet integrity checks. The link layer CRC is transparently generated and checked in the data link layer of the link partners. The header CRC is checked at every hop along the path. The Payload CRC (PCRC) is generated by the source end point and checked at the receiver end point. It provides end-to-end integrity checks and error notification.

Switch elements that forward packets do not have to implement PCRC. In addition, ASI packets use a header CRC that can be checked on a per hop basis by switches as they forward packets. If a header CRC error is detected, the packet is discarded at an intermediate switch or at the terminus of the packet and an ASI route header error is signaled.

Summary

A summary of the comparison of the three fabric standards is shown in Table 1 (page 38). Each of the new standard serial interconnects offers developers a unique set of capabilities. The distinct characteristics of protocol support, flow control, congestion management, and error detection and event handling offer designers advantages for different applications.

System designers must also consider each technology's ability to exploit its underlying infrastructure and leverage the economies of scale before they select a solution for their application. The ecosystem surrounding a given technology will have a profound impact not only on its end cost, but on the speed of its eventual adoption. For example, the flourishing PCI Express ecosystem may make Advanced Switching (ASI) an attractive choice for a large number of applications. **ECD**

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	InfiniBand	SRIO/RapidFabric	ASI
Maximum bandwidth (after 8B/10B encoding overhead)	24 Gbps	10 Gbps	64 Gbps
Lanes supported	x1, x4, x12	x1, x4	x1, x2, x4, x8, x12, x16, x32
PHY speed	2.5 Gbps	1.25 / 2.5 / 3.125 Gbps	2.5 Gbps
Packet types	Reliable connection Reliable datagram Unreliable connection Unreliable datagram Raw IPv6 datagram Raw Ethernet packets	Read Write Sequenced write Atomic operations Maintenance operations Messages Data streams	Tunnels any packet and any protocol Simple Queuing (SQ) Simple Load/Store (SLS) Sockets Direct Transfer (SDT) Multicast Data Streaming and SAR Management packets (PI-4: device management, PI-5: event management, PI-1: congestion management)
Data movement model	Datagram, Streams, RDMA	Load/Store, Messaging	Load/Store, Messaging, Queuing, RDMA
Maximum payload	4096 bytes	256 bytes	2176 bytes
Transaction layer overhead	High, header overhead as high as 126 bytes	Small, 12 to 16 bytes	Small, 12 or 16 bytes
Reliable transport	Yes	Yes	Yes
Multi-cast	Yes	Yes	Yes
Routing	Device-based routing	Device-based routing	Path-based routing
Class of Service	16 Service Levels or Traffic Classes mapped to 16 Virtual Channels	Three transaction requests mapped into four priorities. RapidFabric enhancements have added more classes of service.	Eight Traffic Classes mapped each to eight Bypass capable, eight ordered, and four multicast independently buffered Virtual Channels.
Flow control	Credit-based, Static rate control	XON/XOFF	Credit-based, Status-based (SBFC), minimum bandwidth scheduler, injection rate limiter.
Error detection	Variant and Invariant CRC	CRC (no regeneration, per hop checking)	Header, Link, and End-to-End CRC
Packet forwarding	Does not provide header CRC for cut-through forwarding. Opportunistic cut-through forwarding could be supported.	Allows cut-through only after checking CRC (16-bit) on receiving 82 bytes of the packet. It is not supported for packet size of 80 bytes or less.	Allows cut-through forwarding after checking Header CRC (7-bit) on receiving eight bytes of the packet.
Fabric management	Multiple Host Channel Adapters (HCAs) competing per subnet. SNMP extension.	Multiple hosts compete	Fabric owner election process via spanning tree.

Table 1



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Embedded device development requires concurrent hardware and software optimization

Today's submicron silicon technology is dramatically changing the nature of embedded device design. Today's embedded devices are much more complex, and they require a rapidly growing body of software to ensure their functionality and make them complete, sellable products.

The very nature of embedded systems requires that hardware and software work closely together. With a traditional sequential embedded device development flow, the hardware is developed first and the software second. For many embedded applications, this approach no longer offers competitive results.

By Rindert Schutten and Thomas Anderson

Sequential drawbacks

There are three major drawbacks to the traditional sequential development flow:

- Designing the device architecture without the ability to run critical system and application software can often lead to suboptimal architectures. This is often confirmed by actual device performance and power consumption measurements.
- The development time for the increasing body of software bundled with the device grows proportionately, resulting in prolonged product development cycles. This increases the project cost while decreasing the eventual revenue return due to later market entry.

- Hardware prototypes and emulation systems are too expensive to provide to each member of the software team, which further prolongs software development.

Concurrent development

To address these problems, customers are transitioning to a project flow where hardware and software is developed concurrently. With a concurrent flow, the software team does not have to wait for hardware prototype or emulation releases since the hardware is concurrently in development.

Instead, concurrent development relies on a virtual hardware prototype – a

high-level, fully functional software model of the target device. The sequential and concurrent development flows and their respective project timelines are shown in Figure 1.

The immediate impact on the project timeline when moving to concurrent development is clear. Software development will be started much sooner and the product will be completed much sooner. Less clear from Figure 1 is the reduced impact on the schedule when inevitable design changes occur.

With a traditional development flow, the impact of the software on the architecture or Register Transfer Level (RTL) synthesis is uncovered very late in the process. If a problem with the architecture is found when testing the software, it can lead to software patches that reduce the product's performance or costly RTL redesign.

With a concurrent development flow, the impact of design changes can often be minimized because engineers run software well before the RTL is fully implemented. When a problem with the architecture is found, minimal changes can be made to the RTL design.

Virtual prototyping

To obtain these benefits, an additional issue must be addressed. With a concurrent flow, the software is developed using a virtual prototype before the full RTL is available.

Therefore, designers need to ensure that the virtual prototype remains functionally equivalent to the RTL under development. If the two models diverge in functionality, a great deal of software redesign may need to be performed once the actual silicon is available.

The remainder of this article explores the requirements for the virtual prototype so that it can serve the needs of both hardware architects and software developers while remaining synchronized with the RTL during the development process.

“Mixed-level modeling optimizes the simulation turnaround time; engineers get the highest simulation performance because they can tune the abstraction level of the model ...”

Virtual prototype development

There are two basic requirements to ensure the success of a virtual prototype:

- The virtual prototype needs to provide architectural insights. This usually means that the virtual prototype uses a cycle-accurate or cycle-approximate

modeling style. The architect needs to be able to analyze the cycle-by-cycle utilization of the common resources (such as buses and caches) to make performance predictions.

- The virtual prototype needs to have sufficient performance so that engineers can run the embedded system and application software. In practical terms, this means that a virtual prototype needs to run at least as fast as a hardware prototype, preferably even faster.

Satisfying these two requirements simultaneously presents a classic design challenge: the tradeoff between accuracy and performance. Traditionally this is a tradeoff made by the developer of the virtual prototype. However, this really is a capability that should be available to the end user of the virtual prototype, whether a software developer who is running and debugging code or a system architect refining the architecture.

Mixed-level modeling

Mixed-level modeling provides this flexibility by allowing virtual prototype users to selectively choose the abstraction level for the entire virtual prototype or for their subsystems and components. Mixed-level modeling optimizes the simulation turnaround time; engineers get the highest simulation performance because they can tune the abstraction level of the model (or parts thereof) to the type of issues they are investigating with the simulation.

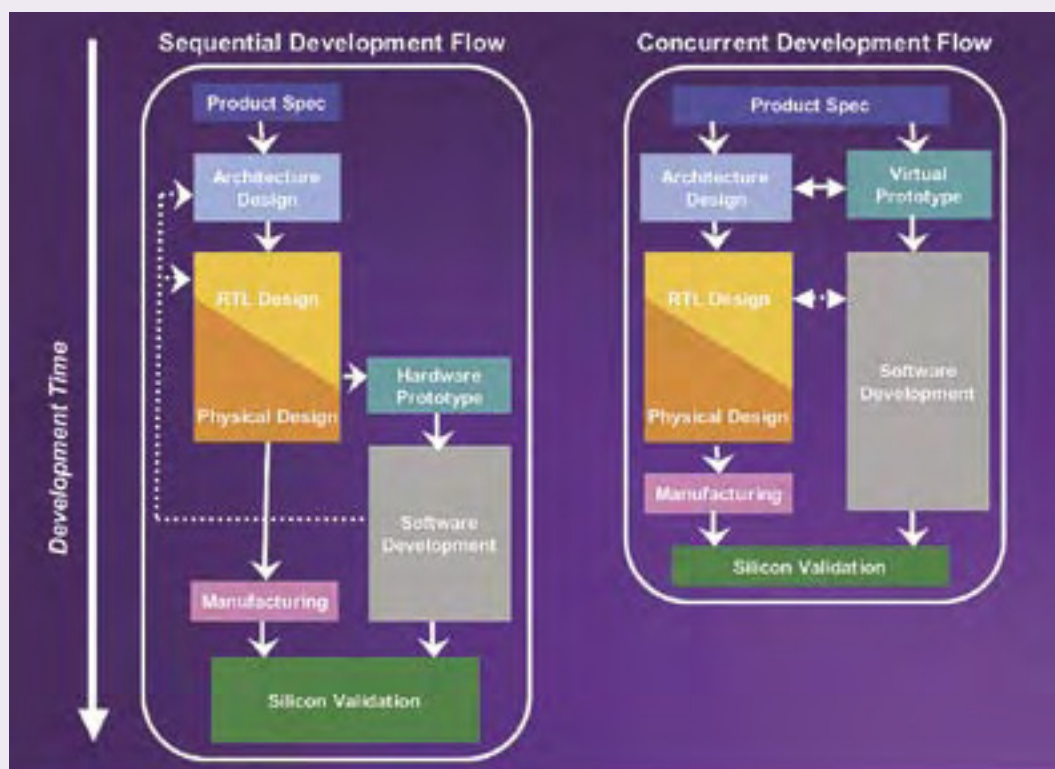


Figure 1

For example, if a particular run does not require architectural detail, then a pure functional-level model of the device should suffice. On the other hand, accurately measuring the performance of a subsystem bus might require cycle-accurate models for that subsystem while simulating the rest of the system at a functional level.

The key to successful mixed-level modeling is a technology that bridges levels of abstractions. Abstraction (by definition) means the omission of detail, which leads to an increase in simulation performance. The question is therefore, “Does a simulation that uses a particular abstraction level provide the answers I need

with sufficient accuracy?" In many cases it will.

For example, typical architectural questions are:

- Do I have enough bandwidth on my bus to carry the on-device traffic?
- Does my choice of processor provide the required performance?
- What is the impact on performance and power if I optimize my software to make fewer memory accesses?

In many cases, simulation can provide answers that are within 5 percent of the actual hardware performance. This is usually acceptable, especially if the virtual prototype provides the option to run the same test on a more accurate model, albeit at a simulation speed that may be orders of magnitude lower. These are precisely the types of tradeoffs that mixed-level modeling provides.

SystemC is a flexible architectural modeling language that facilitates mixed-level modeling. Particularly powerful is its concept of separating communication from function. Based on a single Application Programming Interface (API), alternative models can be created and used to model communication infrastructure.

Mixed-level modeling example

In a demonstration project, two abstraction levels for an on-device bus were implemented – a cycle-accurate interconnect model and a pure functional interconnect model (Figure 2).

This on-device bus is used in a small system with two masters (M1 and M2) and two slaves (S1 and S2). This mixed-level model is configured such that all communication between M1 and S1 is performed in a cycle-accurate fashion, and all communication between M2 and S2 is performed in a fast, functional, untimed fashion. The *bridge model* ensures communication between the cycle-accurate domain and the functional domain by providing a cycle approximation of the functional model.

There are trade offs with this system. For example, the communication between M1 and S2 will be functionally accurate but not cycle accurate. If M1 retrieves data from S2, the latency may not be exact. Similarly, if M2 requires data from S1 the response may not be as immediate as it would be for data retrieved from S2.

The power of this solution lies in that fact that all the functional models (M1, M2, S1, and S2), use the same API irrespective of whether they are connected to the cycle-accurate model of the bus (the architecture domain), or the functional model of the bus (the functional domain).

With mixed-level modeling, users can quickly configure the system as fully cycle accurate, or as partially cycle accurate with higher performance, or as fully functional with all the components connected to the functional model of the bus for highest performance. In the actual implementation of this project, the full-functional model runs about 50 times faster than the completely cycle-accurate model.

Regardless of the level of abstraction, the user can run the same tests and software on all permutations. This allows a software engineer to develop a software component on a pure functional model with a very fast turnaround time. Then, a system architect can explore the impact of the software component on the architecture by using the much slower cycle-accurate interconnect model. The architect can tune the architecture to maximize system performance or provide feedback to the software developer on how to optimize the software for better performance.

Moving to the RTL implementation

The virtual prototype establishes an environment that can satisfy the needs of the hardware architect for accuracy and the needs of the software developer for speed. In addition, this environment satisfies another essential requirement for an effective hardware/software development flow. The virtual prototype also provides the means to ensure the architecture and the RTL model of the target system will

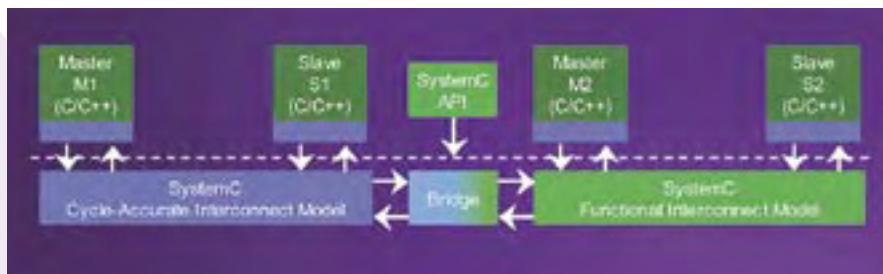
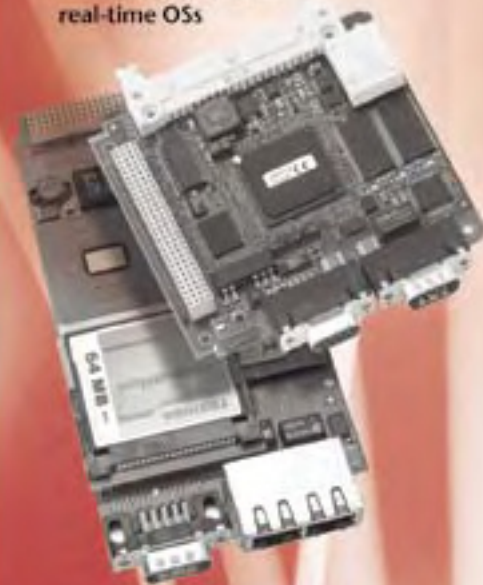


Figure 2

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remain consistent with the software model throughout development.

Being able to run the same tests (including binary compatible software) on both the architecture model and the functional model enables the engineers to craft a set of regression tests. These tests need to pass on both models of the target system and will capture any discrepancy that may occur when the architecture is refined or the RTL implementation diverges from the intended architecture.

Typically this refinement is an incremental process. With the architectural model being cycle-accurate, individual blocks (such as M1 and S1 in Figure 2) can be replaced by actual RTL implementations one by one, until ultimately the complete system is represented by RTL. At the same time, tests running on this mixed-level model capture any discrepancy with the functional model that may occur during this process.

Clearly the set of tests has to be crafted carefully, and the amount of software that can run on an RTL model is limited. However, with the methodology in place and the careful creation of regression

tests, project engineers have the means to ensure model consistency across multiple abstraction levels.

The virtual prototype also enables better implementation decisions for the RTL design. The architect can provide feedback to the designers on how to optimize their RTL for better performance in parallel with similar feedback to the software developers. Thus, architecting the device with the ability to run critical software allows both the hardware and software to be optimized in parallel during their concurrent development. The result is an optimal balance of system architecture, software, and RTL implementation.

Summary

The software content for embedded device designs is rapidly increasing, necessitating a concurrent hardware/software development flow. This need is met by mixed-level modeling which facilitates a true concurrent hardware/software development flow. A virtual prototype satisfies all requirements for such a flow:

- It provides the accuracy that architects need to make their architectural

tradeoffs to optimize performance by using a cycle-accurate model of the target system.

- It provides a fast functional model of the target system for software developers so that they get the fastest turnaround time.
- It allows blocks to be replaced by RTL as the implementation is completed, verifying the hardware in the same environment.
- It ensures that all models are mutually consistent because the same tests and software run on all models irrespective of their abstraction level.

The single environment shared by the hardware and software developers creates a solution where the impact of the software on the hardware can be fully analyzed while both are simultaneously optimized, thereby substantially decreasing the development time for software-rich embedded devices. **ECD**

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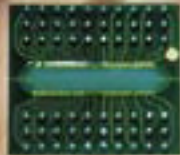
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Rich graphical interfaces for remote embedded applications

By Nate Smith

Remote access to embedded applications over the Internet for monitoring or control provides many benefits for the end user including cost and timesavings. With an Ethernet connection and Internet access, the distance barrier that was once limited to the length of a cable is now removed. Graphical interaction can now be achieved remotely with a minimum of development effort and hardware cost, and the embedded application can be accessed worldwide from any browser.

The need for graphical interfaces

Human interfaces for embedded applications have been developed to adjust, monitor, or control the application within its given environment. Many applications in today's world still make use of simple knobs, switches, buttons, or lights for feedback and human intervention. As applications have advanced in complexity due to normal product evolution and technology change, interfaces have advanced to

meet market sophistication requirements. As a result, menu-based Graphical User Interfaces (GUIs) provide the intuitive, necessary interface.

Graphic display interfaces provide many benefits. For the manufacturer, they can be used to simulate configurations and maintain the ability to add or change features. Advanced interfaces allow for many product changes or updates without necessarily requiring hardware

modification. For consumers, graphical interfaces provide an intuitive method for configuring their preferences, on demand.

Interface costs

While there are many advantages to integrating a GUI into an application, the integration of a physical interface can become cost prohibitive. An LCD display/touchscreen with a supporting 32-bit color LCD controller and an RTOS for a legacy application that requires appropriate timing

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SMT287

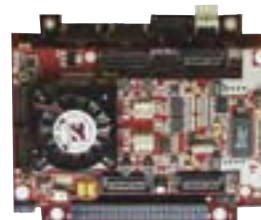
PC 104 Disk Storage Solution



This is an example unit made up of SMT130 carrier and SMT387 module with 'C6415 DSP; Virtex II VP20; SATA Link; and Rocket Serial Link (RSL). In this solution the DSP can directly write to or read from Serial ATA hard disk supporting FAT32 filing system.

SMT290-VP7-5

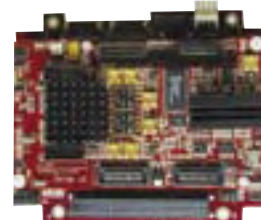
PC 104 two channel ADC



An ADC Module with 2-Channels of each sampling at 210MSPS @ 12bits. This is the first DAQ module to use a Virtex-II Pro FPGA and a unique 'Double-Decker' inter-connections concept that separate the Digital control functions from the noise-sensitive DAQ semiconductors.

SMT291

PC 104 two channel ADC



Built on the SMT391 module this combination provides a two channel ADC sampling at 1GHz per channel with 8bits resolution.

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A TRULY SCALABLE SOLUTION

control can significantly burden the cost of an application.

Another downside for GUI integration into an application is that development time can be impacted. This is particularly true if the appropriate resource skill is not available in house.

The risk of increased development time can be negated through the use of graphical development kits such as those offered by Amulet Technology and EarthLCD. The kits can save development time and facilitate the production of a high quality product. Kit contents commonly include a graphics operating system, a controller board, and an LCD or touchscreen display.

Unfortunately, many deeply embedded products are too cost-sensitive to justify the extra development and recurring application costs needed for an integral LCD and touch panel, even with all of the advantages of a graphical interface. As an alternative, remote graphical interfaces using a served Web page can be created for remote PCs, PDAs, or cell phones that significantly reduce the cost burden to the application.

Cost effective interface

Remote interfaces based on served Web pages are soon to see significant enhancements in graphical content, particularly for 8-bit microcontroller applications that hold the predominant position in the industry. For these applications, the achievement of a remote, graphically rich interface is quite compelling.

Historically, the program memory for 8-bit microcontrollers has limited the interface to text, very simple graphics, and toggle action icons. For instance, the Microchip PIC16 family used in combination with an ultra-lean Iosoft TCP/IP stack implementation is suitable for installation on products based on low cost microcontrollers. The software makes it possible for embedded systems to provide HTML Web pages via an Ethernet LAN/WAN connection. An example is of a Web page GUI is shown in Figure 1.

New interface solution

Imagine the graphical content that could be possible if the microcontroller had significantly more program memory available for an interface. With this development, graphics could be easily added without compromising application features.

Maintaining its cost effectiveness, Microchip recently introduced the high-density 8-bit PIC18F87J10 microcontroller family (Table 1). With up to 128 KB of flash program memory and a rich set of peripherals, the Microchip PIC18F87J10 in combination with the newly introduced ENC28J60 bridge device (more on that later) can serve a rich, graphical Web page providing the benefits of remote application access while enhancing the user experience.

Microchip TCP/IP stack

Communication over the Internet is accomplished through the implementation of a TCP/IP stack that is optimized for the PIC18 microcontroller. The TCP/IP stack, furnished free of charge by Microchip, is a suite of programs that provides services to standard or custom TCP/IP-based applications (Figure 2).

Based on the TCP/IP Reference Model, Microchip’s TCP/IP stack is divided into multiple layers, where each layer accesses services from one or more layers below it. Per specifications, many of the TCP/IP layers are live in the sense that they not only act when a service is requested, but also when events like time-out or new packet arrival occur. The stack is modular in design and was written in the C programming language. Effective



Figure 1

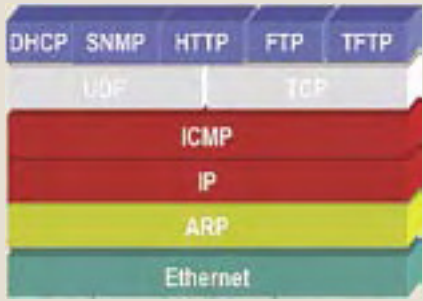


Figure 2

Max. Speed	Packages	Operating Voltage	Program Memory	SRAM Data Memory	I/O	ADC Ch.	Comp.	INTOSC	Serial I/O
40 MHz	64 or 80-pin TQFP	2.0 to 3.6 V	Up to 128 KB	Up to 4 KB	Up to 66	Up to 15x 10-bit	2	32 kHz	2x EUSART, 2x M ² C/SPI

Table 1

Max. Speed	Packages	Operating Voltage	MAC	PHY	TX/RX RAM Buffer	Interrupts	LEDs	Temp. Range	Serial
25 MHz	28-pin SPDIP, SOIC, SSOP, QFN	3.3 V	Yes	Yes	8 KB	2	2	–40 to +85°C	SPI

Table 2

SMT118

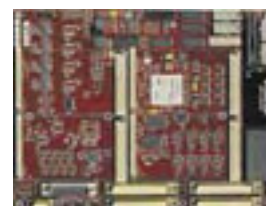
Stand Alone Module Carrier



Responding to increasing demand for portable and embedded DSP solutions brought about SMT118, a truly 12V-Input stand-alone carrier. The SMT118 has been developed to carry 3 Modules and attention to power-management enables it to be powered by a small battery source! The SMT118-T is lower cost version with less I/O pins.

SMT148

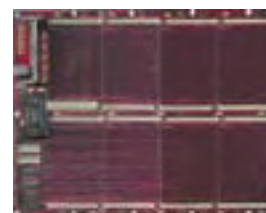
4 sites stand alone module carrier



The SMT148 carrier has 8 on-board channels of 400KHz analog inputs and outputs, three UART connections (one RS485 and two RS232), 56 pairs of LVDS connections, JTAG Debugging, an RSL, an SHB, two USB's and two FireWire (1394b) ports. There are 32 LEDs connected to the VirtexII Pro to enable a display.

SMT180

8 sites stand alone module carrier



The SMT180 is an extension of the path created by SMT118. The SMT180 has taken the step of Stand-alone operation to another level as two SMT180s can be cascaded and provide a platform for no less than 16 Modules. If each module were an SMT374 it would offer in excess of 40GFlops of DSP Processing that can be integrated into a 0.5 cubic meter box and run from a car battery and still keep cool.

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"Remote interfaces based on served Web pages are soon to see significant enhancements in graphical content, particularly for 8-bit microcontroller applications that hold the predominant position in the industry."

implementations can be accomplished with roughly 20 KB of code, which leaves plenty of code space to serve graphical Web pages.

Microchip Ethernet controller

Microchip Technology's new 10Base-T standalone Ethernet controller comes with an 8 KB dual-port SRAM buffer and a Serial Peripheral Interface (SPI) in a 28-pin package. The specifications are shown in Table 2, and a block diagram in shown in Figure 3.

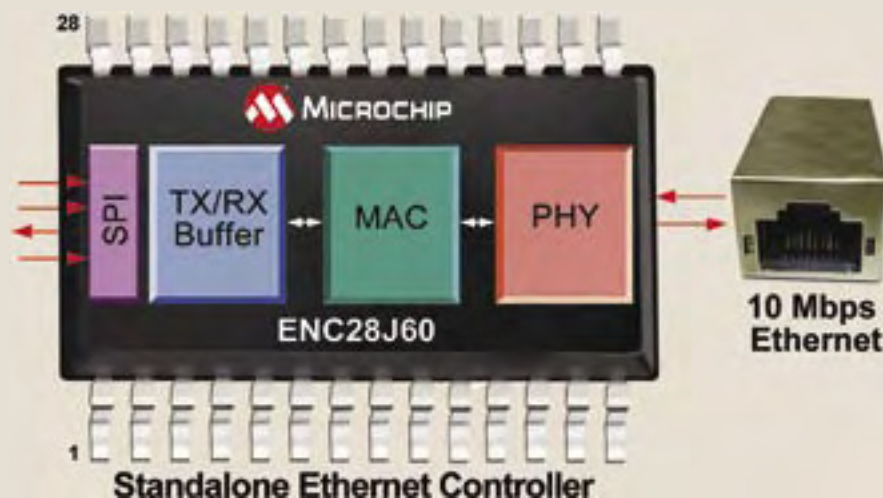


Figure 3

So why did Microchip develop the ENC28J60 Ethernet controller? The answer is actually quite simple. Embedded designers who require application access for remote control or monitoring are often faced with the complexity of expensive Ethernet controllers with a large footprint that are tailored for personal computing systems.

While most Ethernet controllers come with greater than 80-pin packages, the IEEE 802.3 compliant ENC28J60 offers comparable features in a 28-pin package, which simplifies the design and reduces the overall occupied board space. Additionally, the ENC28J60 Ethernet controller employs the industry standard SPI serial interface that requires only four lines to interface to a host microcontroller.

The SPI interface, small footprint, and equally small price tag (\$4.17 each in 10Ku) for this Ethernet controller has opened the door for network enabling low cost applications and displacing expensive integrated application interfaces.

Application example

Many applications can use a remote graphical interface, such as the hotel application shown in Figure 4 (page 51). With the described microcontroller and Ethernet controller solution, the hotel front desk can gain the capability to access pertinent controls and sensors from individual rooms over an Ethernet network.

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If Ethernet-enabled hotel room controllers are placed in each room, remote motion detection, mini-bar inventory, lighting control at checkin or checkout, privacy indication, and access control could all be accomplished remotely via a nice graphical interface displayed with a standard Web browser.

Given the number of controls or sensors in this example, a graphical interface in a centralized, remote location would greatly enhance the user experience and the ability to effectively manage multiple hotel rooms remotely. This would also provide for improved customer service and peace of mind concerning safety and security while improving accuracy through real-time billing.

Ethernet-Enabled Hotel Room Controller

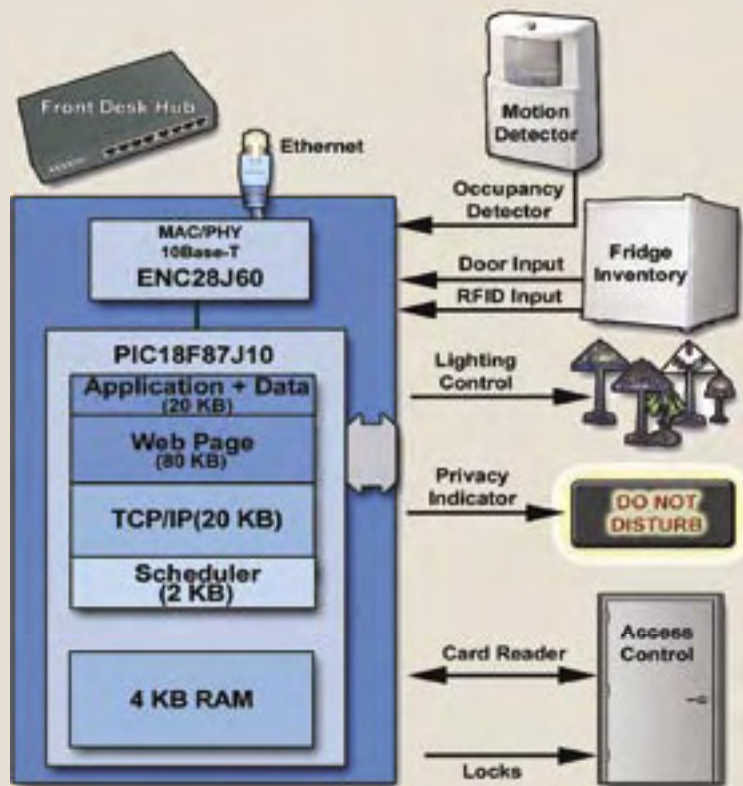


Figure 4

Summary

The Microchip ENC28J60 Ethernet controller provides a low cost, small footprint Ethernet interface for embedded applications. When combined with cost effective, high-density 8-bit microcontrollers like the Microchip PIC18F87J10, expensive graphical interfaces that are resident on the application can be replaced with a remote graphical interface. The remote GUI Web page can be created inexpensively using any readily available standards-based HTML software package. Remote graphical interfaces maximize efficiency for management capability, and save development time and cost. **ECD**

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GDD8000



GDD600 Floating Point computation on Fixed Point TMS320C6000. A set of over 100 functions and macros for DSP operations like FFT, Fast Hartley Transform, FIR/IIR filters, vector, complex number arithmetic, and data conditioning (spectral windows). These are performed on the IEEE-754 Floating Point format. A set of data conversions functions is available to convert FP data to/from integer and Q15 fixed-point formats. Unlike other libraries in the market all GDD libraries are fully interruptible and re-entrant. With a single instance of any function linked in, all application threads can make a call to it simultaneously.

GDD8000 Hand coded EISPACK library for solving eigenvalue/eigenvector problems on TMS320C6000. The library is a set of about 100 functions and macros that find a solution to a linear algebraic eigensystems with various matrices, real or complex, general, band, symmetric or Hermitian. All or selected eigenvalues and eigenvectors can be computed. Several types of matrix decompositions like SVD or QR are performed by the library functions.

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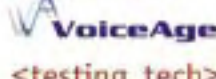
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Standard mezzanine interfaces facilitate outsourcing for TEMs

Mezzanine interfaces like PMC, Processor PMC (PrPMC), and AdvancedMC (AMC) simplify telecom blade design and reduce cost by eliminating the need to design a custom blade for every application. In this article, Todd describes the evolution of mezzanine cards and their benefits to telecom OEMs.

By Todd Wynia

increasingly important as TEMs continue to downsize their engineering staffs.

Control upgrades

Control, an integral part of every telecom infrastructure application, is a perfect example of a function that requires periodic upgrades, and a prime candidate for outsourcing. By implementing their control subsystem on a mezzanine card, TEMs can perform significant control upgrades (such as adding a faster processor or memory) with little or no disruption to the rest of the blade.

Application-specific blades

By combining a generic carrier blade (such as PICMG 2.16 or AdvancedTCA) with mezzanine-based networking, signal processing, mass storage, and I/O functions, blade suppliers can quickly create a broad range of application-specific blades with a handful of general purpose components. The proprietary telecom gateway example shown in Figure 1 features the following:

- Processor PMC (PrPMC)
- PCI Telecom Mezzanine Card (PTMC)
- Plain Old Telephone Service (POTS) phone
- Public Switched Telephone Network (PSTN)
- Session Initiation Protocol (SIP) clients

Development savings

Telecom Equipment Manufacturers (TEMs) are also embracing the mezzanine concept as a way to reduce design time and cost, particularly TEMs who are utilizing proprietary pizza box (no standard back-plane interface) blades. Adding standard mezzanine interfaces to these otherwise proprietary blades enhances flexibility and reduces cost by enabling TEM to upgrade portions of their systems without redesigning entire blades.

Equally important, it makes it easier to outsource (or acquire off-the-shelf) a broad range of functionality that would otherwise have to be designed exclusively in-house. This outsourcing capability is becoming

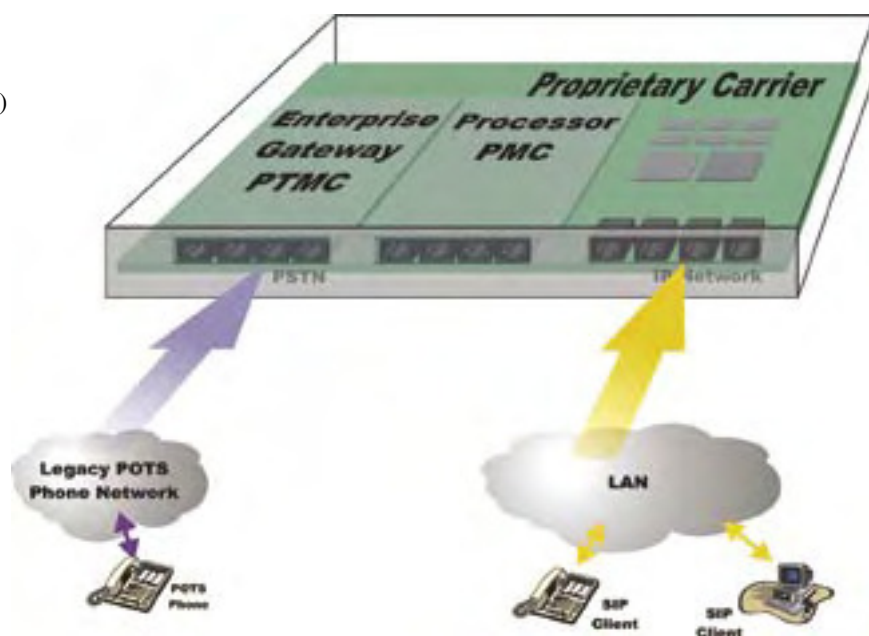


Figure 1

Third party benefits

The mezzanine implementation also gives TEMs ready access to off-the-shelf control solutions from blade suppliers, enabling them to delegate the responsibility for control design, obsolescence, and maintenance to third party vendors. All told, TEMs can typically shave up to 50 percent off of their design times by purchasing their control solution off the shelf instead of designing it in house. At the same time, they can also reduce ongoing life cycle maintenance costs by 60 percent or more.

PMC, PTMC, and PrPMC

The PMC was one of the first standard

mezzanine interfaces to achieve a measure of popularity in the telecom industry, especially among designers of VMEbus- and CompactPCI-based shelves. Utilizing the same electrical interface as PCI, PMC was desirable because it gave mezzanine designers access to the same low-cost production components used in desktop PCs. The drawback to PMC is that it uses the PCI bus for both control and data transfer operations, thereby creating a potential bottleneck for applications requiring high data throughput or timely control response.

PTMC, a telecom-friendly extension of PMC, solved this problem by adding

support for a separate data bus that could accommodate TDM, Ethernet, ATM, and Packet Over SONET (POS) data formats. This high-bandwidth data plane made it possible for modules to send and receive TDM data or packets directly while also conducting control operations via the PCI bus. PTMC is the mezzanine of choice for PICMG 2.16 systems, but is also gaining a following among suppliers of AdvancedTCA blades.

The PrPMC is an extension of PMC that enables CPUs residing on the PMC mezzanine card to act as the main processor for the host carrier card. PrPMC accomplishes this by redefining some existing PMC pins and adding new definitions to previously reserved or obsolete pins. These additional/redefined pins enable the PrPMC interface to support 66 MHz data transfers and provide enhanced interrupt handling capabilities, which is essential for having the PrPMC CPU act as the master/host processor. PrPMC also provides relaxed height restrictions, which enables it to accommodate high profile components such as heat sinks, fans, power supplies, and SODIMM memory modules.

Future implementations of PMC and PrPMC are likely to de-emphasize the PCI interface, focusing instead on higher speed packet interfaces. These packet interfaces, which will be used for both the control and data planes, will improve throughput and simplify design by eliminating the need to translate between PCI and packet data formats.

PrPMC example

A number of companies offer PrPMC modules. For example, the Artesyn PmPPC7447 (Figure 2) features the following:

- 1 GHz Freescale PowerPC MPC7447A
- AltiVec vector processor
- 32 KB of on-die L1 cache
- 512 KB of on-die L2 cache
- 2 GB of external memory
- Two Gigabit Ethernet (GbE) ports
- An I2C bus system management controller



Figure 2

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The PmPPC7447's high speed CPU and memory subsystem make it an ideal control plane processor for optical and wireless infrastructure. Its AltiVec vector processor and dual-channel GbE interfaces also make it well suited for augmenting packet processing and routing performance in voice gateways, and for enhancing protocol processing performance in SS7 and SIGTRAN signaling control points and gateways.

AMC benefits

The PMC installed base will likely make it a popular mezzanine option for some time to come. Meanwhile, a faster packet-based telecom mezzanine interface is emerging. AdvancedMC offers higher bandwidth, field replaceability, a larger form factor, higher power handling capability (up to 60W), and integrated system management. These features make AdvancedMC ideal for designing a complete high performance CPU or DSP subsystem that can handle both control and packet processing on a single module.

As an example, the Artesyn KosaiPM shown in Figure 3 features the following:

- Intel Pentium M running at up to 1.4 GHz
- Full-height PICMG AMC form factor
- Up to 2 GB DDR DRAM with ECC
- Dual GbE connectivity to baseboard
- PCI Express connectivity to baseboard
- Full hot swap support
- USB and Console serial ports via front panel
- Intelligent peripheral management functionality
- Carrier Grade Linux support



Figure 3

The AdvancedMC high speed packet-based serial interface provides up to 21 I/O channels, each capable of operating at 12.5 Gbps. This bandwidth enables the modules to move data to and from the baseboard (and other AdvancedMC modules) at speeds of up to 200 Gbps, five times that of the SONET OC-768 standard. AMC modules are also protocol agnostic, giving TEMS tremendous flexibility in how they handle communications between

the AMC module and the carrier. Ethernet is the default protocol, but AdvancedMC modules can support any number of protocols including PCI Express, Rapid I/O, and InfiniBand.

AMC field replaceability

With respect to traditional mezzanine interfaces like PMC, one of AdvancedMC's most significant enhancements is its hot swappability. Unlike other mezzanine modules, which must be bolted on at the factory, AdvancedMC modules are field replaceable.

This capability increases system availability by enabling service providers to service, upgrade, and replace individual modules without taking entire blades off line. It also reduces the cost of provisioning systems, enabling service providers to bring functionality on line with a finer degree of granularity based on actual subscriber demand. AdvancedMC's field replaceability reduces capital expenditures by enabling service providers to stock and replace individual modules rather than entire blades.

AMC management

Another feature that makes AMCs very attractive to TEMs and service providers is its integrated system management.

AdvancedMC modules provide an on-board I2C-based Integrated Peripheral Management Interface (IPMI).

This interface enables shelf management that monitors and controls individual modules (Figure 4). This capability greatly enhances availability and serviceability by enabling shelf management to pinpoint faults and take corrective action at the module rather than blade level.

"AdvancedMC offers higher bandwidth, field replaceability, a larger form factor, higher power handling capability (up to 60W), and integrated system management."

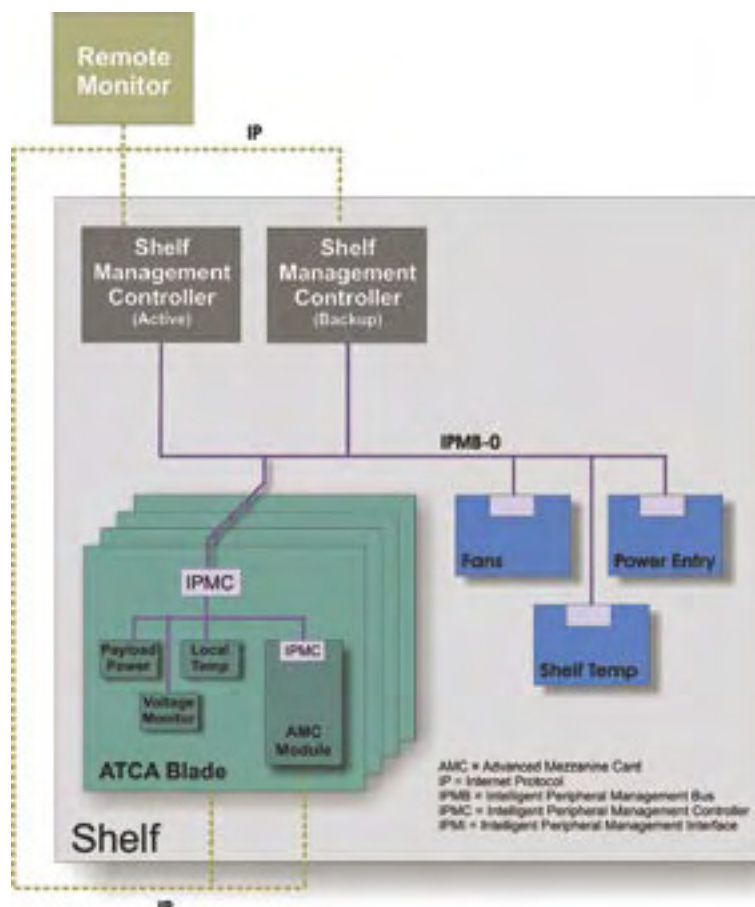


Figure 4

AMC costs

AdvancedMC's increased performance and flexibility, not surprisingly, comes at an increased cost. First, because AMC modules are field replaceable, they require a ruggedized card-cage style connector that can withstand module insertion and extraction in the field. AdvancedMC's hot swap functionality, higher bandwidth, and integrated system management requires additional circuitry, which also increases cost.

Still, for many TEMs, this incremental cost increase is more than offset by reductions in operational expenditures made

possible by AdvancedMC's enhanced performance, availability, and serviceability.

AMC applications

While control is one of the most common uses for mezzanine solutions, mezzanine modules can also be used to add auxiliary packet and media processing subsystems such as DSP farms, as well as a variety of I/O, WAN, and LAN interfaces. AdvancedMC's large form factor, high power handling capability, and high speed packet interface make it particularly well suited to implementing complex subsystems that offer multichannel

WAN interfaces and multiple CPU/DSP packet/media processing complexes.

AdvancedMC's hot swappability and integrated system management also make it ideal for building scalable, field replaceable systems that can be expanded, serviced, and upgraded with maximum availability and efficiency.

AdvancedMC modules make it easy to create scalable high-density blades dedicated to a specific function such as control, SIGTRAN signaling, transcoding, interfacing, or packet processing. The versatile modules also make it easy to combine multiple functions on a single blade and alter the mix as applications and/or system partitioning changes. Either way, they can spread critical functions across multiple field replaceable modules in a way that maximizes scalability, upgradeability, availability, and serviceability.

AMC example

A single-board media gateway implemented with an AdvancedTCA card equipped with AdvancedMC modules is shown in Figure 5.

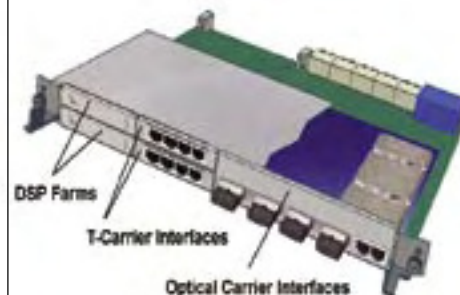


Figure 5

The gateway receives TDM voice traffic via a SONET or T1/E1 interface, passing the voice channels to DSP farm modules for transcoding and packetization. The gateway then transports the packetized voice off the board via the high speed IP switch fabric interface. Alternative solutions could be architected using a multi-blade approach, dedicating one blade to DSP transcoding and packetization, and another blade to the provision of the TDM interfaces.

MicroTCA

Though originally developed as a field replaceable mezzanine expansion interface for AdvancedTCA blades, AdvancedMC is poised to become the foundation for a new small form factor shelf architecture targeting low to midrange high availability telecom applications. Known as MicroTCA, the proposed hot-swappable architecture defines a rack-mountable

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4U shelf populated with AdvancedMC modules.

MicroTCA eliminates the need for an AdvancedMC carrier, enabling TEMs to plug AdvancedMC modules directly into a standard 19 inch shelf measuring 4U by 300 mm deep including cabling (a key requirement for optical applications). The resulting system costs less and occupies less space than a comparable AdvancedTCA/AdvancedMC system, and enables TEMs to leverage the installed base of off-the-shelf AdvancedMC modules. It also enables TEMs to utilize the same serial packet interface and integrated IPMI system management used in AdvancedTCA/AdvancedMC systems.

MicroTCA backplanes will provide scalable bandwidth up to 40 Gbps, and support star, dual-star, and full-mesh topologies. They will also be protocol agnostic which enables them to support a variety of packet-based protocols including Ethernet, PCI Express/ASI, and Rapid I/O. MicroTCA shelves will be able to accept up to 48 standard AdvancedMC modules in a variety of form factors, including half-height/single-wide, half-height/double-wide, full-height/single-wide, and full-height/double-wide. The shelves will deliver 12 V power with power consumption for individual modules ranging from 20 W (half-height/single-wide) to 60 W (full-height/double-wide).

To enhance availability, MicroTCA shelves will support hot-swappable AdvancedMC modules, which will enable service providers to replace individual modules in the field without taking the entire shelf off line. The MicroTCA backplane will also provide I2C-based IPMI, which will enable shelf management to monitor and control each module installed in the backplane.

MicroTCA's compact form factor, scalable bandwidth, and low-cost make it a perfect complement to AdvancedTCA shelves for a wide range of cost and space constrained telecom applications. Among these are pole-mounted Base Transceiver Stations (BTSs), Digital Subscriber Line Access Multiplexers (DSLAMs), Fiber-To-The-Curb (FTTC) units, workgroup routers, converged home networks, voice gateways, edge routers, and optical multiplexers.

Summary

With time-to-market and cost pressures bearing down on them, TEMs are moving aggressively towards outsourcing basic infrastructure such as backplanes, control, and I/O. Standard mezzanine interfaces like PMC, PrPMC, and AdvancedMC make outsourcing simple and economical, enabling TEMs to focus their scarce engineering resources on value-added functionality such as application software and services. **ECD**

Todd Wynia, VP Marketing, Artesyn Communication Products. Todd has more than 18 years of experience in the embedded computing market, and regularly contributes his experience to the organizations that drive the telecom standards. He holds a BS in Economics from the University of Wisconsin.



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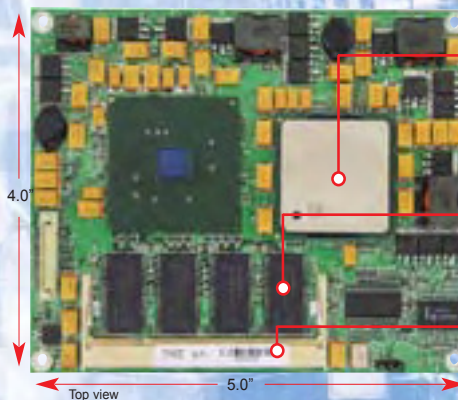
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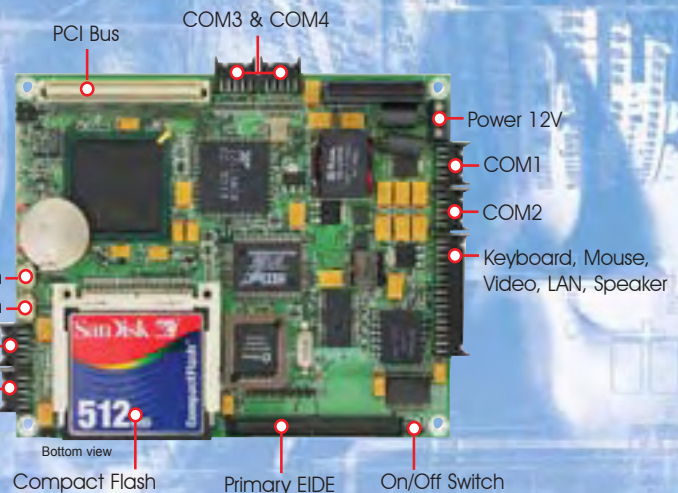
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SODIMM socket

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Company name Model number	Description/Website
Artesyn Communication www.artesyncp.com	
AM7501	A Pentium M-based Advanced Mezzanine Card • Provides the ability to add processing power to AdvancedTCA or proprietary systems equipped with AMC expansion bays • Suitable as a control plane processor for optical and wireless infrastructure, for augmenting packet processing and routing performance in voice gateways, and for enhancing protocol processing performance in SS7 and SIGTRAN signaling control points and gateways • Single-wide, full-height AMC card that can be used with an AdvancedTCA or proprietary carrier card that provides AMC bays • Optimized for embedded control • 1.6 GHz Pentium M processor with a 400 MHz, 3.2 Gbps front-side bus, 1 MB of L2 cache, and SIMD extensions • Server-class E7501 North Bridge • Up to 2 GB of ECC SDRAM • 64-bit PCI-X bridge provides access to two Gigabit Ethernet channels, up to 128 MB of Flash memory, a USB interface, an I2C system management interface, and a front-panel 10/100Base-T management interface • Communicates with AdvancedTCA carrier cards via the two Gigabit Ethernet channels, which are routed to the AMC connector • Supports Carrier Grade Linux
KosaiPM	Intel Pentium M • Full-height PICMG AMC form factor • Up to 2 GB ECC DRAM • Dual Gigabit Ethernet connectivity to baseboard • PCI Express connectivity to baseboard • Full hotswap support • USB and Console serial ports via front panel • Intelligent peripheral management functionality • Carrier Grade Linux support
KosaiPM AMC	An AMC module based on the Intel Pentium M processor, providing a complete processor subsystem • Allows communication equipment manufacturers to add modular and upgradeable compute functionality to their AdvancedTCA or proprietary baseboards and provide the localized horsepower necessary for applications such as protocol processing, packet processing, data management, and I/O management • Supports high-speed packet data transfers on and off the card with PCI Express and dual Gigabit Ethernet interfaces to the baseboard • Hot-swappable • IPMI-based system management interface • Intel Pentium M running at up to 1.4 GHz • Full-height PICMG AMC form factor • Up to 2 GB DDR DRAM with ECC • Dual Gigabit Ethernet connectivity to baseboard • PCI Express connectivity to baseboard • Full hot swap support • USB and console serial ports via front panel • Intelligent peripheral management functionality • Carrier Grade Linux support
BittWare www.bittware.com	
B2-AMC	An Advanced Mezzanine Card that supports universal baseband processing for any 2G, 2.5G, or 3G wireless application • Full-height, single-wide AMC • Six ADSP-TS201S TigerSHARC DSPs • Xilinx Virtex-II Pro FPGA (XC2VP20/30/40) for I/O, routing, and processing • Network interface via AMC connector • Network switch fabric interface via Virtex-II Pro 4x RocketIO • Configurable to support: Serial RapidIO, PCI Express and Advanced Switching, Aurora, and XAUI (10 GbE), GigE • Antenna interface • General-purpose I/O and JTAG port on front panel • Module management control implementing IPMI • System synchronization via AMC system clocks • Booting of DSPs and FPGAs via nonvolatile Flash memory • Control interface via 10/100Base-T for command, control, and reprogramming
Kontron www.kontron.com	
AM4001 (Pentium M)	AMC processor module, single-width – half/full height • Intel Pentium M, scalable up to 2.0 GHz • Max 4 GB memory • Flexible Gigabit and PCI Express fabric interface • Superb monitoring features • PICMG AMC.0/.1/.2/.3 compliance • IPMI v1.5 support • PCI Express interface • 2 GbE 1000Base-BX (SerDes) ports
Motorola www.motorola.com/computers	
AXP Advanced Switching Platform	An application-enabling platform • Shelf capable of 240 Gbps of switching capacity (PICMG 3.2 InfiniBand) • Comprehensive software suite • Management software (IPMI, Web, SNMP) • Variety of payload blades • Support for AMC sub-module standard
SBS Technologies www.sbs.com	
TELUM 1001-03M	An Advanced Mezzanine Card for Asynchronous Transfer Mode (ATM) communications • Provides full-duplex OC-3 ATM front I/O capabilities to an AdvancedTCA system • Intel 41210 serial-to-parallel PCI bridge to the PCI Express bus to communicate with the host processor on an AdvancedTCA system • Complies with ATM Forum UNI 3.1 and TM 4.0 and is based on an advanced ATM Segmentation And Reassembly (SAR) controller designed to optimize the PCI Express bus interface • IPMI subsystem • Hot-swappable and field-replaceable
Yamaichi Electronics www.yeu.com	
AMC (CN074 Series) Connector	PICMG AMC Revision 1.0 compliant • GR-1217-CORE compliant • Compression style contacts to the carrier board with wiping action to ensure high reliability • Integrated, high-performance Yamaichi developed YFlex with interconnect technology • Base substrate is LCP material, which has a very low CTE • Contacts designed for high-speed applications – very short stub • Supports speeds beyond 12.5 Gbps • Operating temperature: -40 °C to 70 °C

Company name Model number	Description/Website
Actis www.actis-computer.com	
PCOM-1870	A Motorola PowerQUICC 2 processor PMC • Quad-channel HDLC controller or E1/T1/J1 ports • Triple Fast Ethernet • 128 MB of SDRAM, 16 MB of Flash • Support 32-bit/33 MHz PCI interface
PLAN-1440	An AMCC PowerPC 440GX at 533 MHz processor PMC • Dual Gigabit Ethernet interfaces, 128 MB of SDRAM, 16 MB of Flash • Supports 32/64-bit, 33/66 MHz PCI interface
Artesyn Communication www.artesynpc.com	
PmPPC2750	A dual-processor PMC card for telecom systems • Two IBM PowerPC 750FX processors at 800 MHz, each with 512 KB of L2 cache • Marvell Discovery GT-64260B PCI bridge with a 133 MHz processor bus • Up to 512 MB of shared SDRAM • Two 10/100Base-T Ethernet ports, two serial ports, 8-channel DMA controller, I2C bus controller • Supports VxWorks and Neutrino
PmPPC440	AMCC PowerPC 440GP system-on-a-chip processor running at 400 MHz • Up to 133 MHz PCI-X interface, backwards compatible with PCI 2.1 • 64 MB, 128 MB, 256 MB, 512 MB or 1 GB DDR ECC SDRAM in SODIMM package • Dual 10/100BaseTX Ethernet interfaces with front bezel access • Processor-PMC Monarch and Non-Monarch modes • Dual serial ports via PMC P14 or single serial port via front bezel • I2C interface • VxWorks and Linux support
PmPPC750f	PowerPC 750FX processor running at 733 MHz • 128 MB, 256 MB, 512 MB or 1 GB ECC SDRAM in SODIMM package • 32/64-bit 33/66 MHz PCI with DMA • Three 10/100 Ethernet interfaces • Processor PMC Monarch and Non-Monarch modes • Two serial I/O ports • I2C interface
DSS Networks www.dssnetworks.com	
Gig-PrPMC Modle 7463	PowerPC based Processor PMC • 833 MHz Freescale MPC8540 PowerQUICC III (up to 1 GHz) • 256 MB DDR333 SDRAM, 16/32 MB Flash • 2X Gigabit Ethernet, 1X 10/100 Ethernet • 1X RJ-45 for 10/100, serial console port • 2X LC SFP connectors for Gigabit fiber and copper applications • 2X quad multifunction LEDs for TX, RX, LINK, and processor STATUS • 64-bit PCI, 133/100/66 MHz PCI-X (64-bit/66 MHz PCI compatible) • 2.15 compliant backplane interfaces for all Ethernet ports • ANSI/VITA 32 Processor PMC (PrPMC) • IEEE-1386 PMC, IEEE 802.3, PICMG 2.15 R1.0, PCI 2.2, and PCI-X 1.0 compliant • Monarch or non-Monarch modes • Internal RapidIO, Interrupt, I2C, DMA, and UART controllers • Ruggedized features include conformal coating and extended temperatures
Embedded Planet www.embeddedplanet.com	
EP425M	A PMC compatible SBC • Intel IXP 425 up to 533 MHz • PMC / PrPMC / PTMC • SDRAM: 64, 128 or 256 MB • Flash: 16, 32, or 64 MB • NVRAM: 256 or 512 KB • 2-10/100Base-T Ethernet • Two RS-232 ports • USB 1.1 (device) • EP X Bus for direct access to IXP 425 • Standalone or PMC mode • JTAG Debug • CD-ROM with design, reference, and complete documentation • Embedded Linux and VxWorks BSPs available • Complete firmware
EP82xxM	Freescale PowerQUICC II PowerPC 8280, 8270, 8266, 8265, and 8250 processors • Can operate as PrPMC or standalone module • PrPMC monarch or non-monarch • PTMC PICMG 2.15 configuration 1 • SDRAM 64, 128, or 256 MB • Flash 16, 32, or 64 MB • Two 10/100Base-T Ethernet • Two RS-232 serial ports • 32-bit, 33/66 MHz PCI bus • UTOPIA 8/16 via PTMC PN3 and PN4 • Debug COP/JTAG • Serial EEPROM I2C • Serial temperature I2C • Serial RTC I2C • Dipswitch 4-position slide switch • BCSR Control and Status Registers • 5.25 to 3.0 VDC single power supply source (1.5A max.) • Mechanical 149 mm x 74 mm • Operating range 0°C to 70°C, extended range -40°C to 85°C available
esd www.esd-electronics.com	
PMC-405	A PowerPC-based PMC module with Ethernet and CAN interfaces • IBM PowerPC 405GP processor at 200 or 266 MHz • 32 MB (optional 64 MB) of SDRAM • Up to 32 MB of Flash • Optional nonvolatile NVRAM • 10/100Base-T Ethernet interface with RJ-45 interface on front panel • Two CAN interfaces, TTL-level signals via PMC I/O connector • One RS-232 via PMC I/O connector and one RS-232 via DSUB9 on front panel
Extreme Engineering www.xes-inc.com	
XPedite1000	A dual Gigabit Ethernet Processor PMC (PrPMC) module • PowerPC 440GX processor at 500 to 800 MHz • 133 MHz PCI-X PrPMC interface • Up to 1 GByte SO-DIMM 333 MHz DDR SDRAM • 4 to 128 MB soldered Flash • 512 KB socketed Flash • Two 10/100/1000Base-T Ethernet ports • Two RS-232 serial ports • Front or rear I/O • Integrated 256 KB SRAM or L2 cache • VxWorks driver and board support package • Linux LSP
XPedite1001	PowerPC 440GX 500-800 MHz processor • Conduction cooled mezzanine card without faceplate I/O • Extended shock and vibration tolerance • 133 MHz PCI-X PrPMC Interface • Up to 512 MB 333 MHz DDR SDRAM • 4 MB Soldered Flash • Two 10/100/1000 Ethernet Ports • Two RS-232 serial ports • Rear I/O • Integrated 256 KB SRAM or L2 Cache • VxWorks Driver and BSP • Linux LSP
XPedite3000	Dual Gigabit Ethernet Processor PMC Module Based on the Broadcom BCM1125 Processor • 64-bit MIPS, 600-800 MHz Processor • 66 MHz / 32bit PCI PrPMC Interface • Up to 1 GB Configurable DIMM 333 MHz DDR SDRAM • 4-64 MB Soldered Flash • 512 KB Socketed Flash • Two 10/100/1000 MBps Ethernet ports • Two RS-232 Serial ports • Front or Rear I/O • Integrated 256 KB SRAM or L2 Cache • VxWorks BSP • Linux LSP
XPedite4000	IBM 750GX PowerPC Processor PMC Module with Two Gigabit Ethernet Ports • PowerPC 750GX 500-1000 MHz Processor • 133 MHz PCI-X PrPMC Interface • Up to 1 GB SO-DIMM 400 MHz DDR SDRAM • 32-64 MB Soldered Flash • 512 KB Socketed Flash • Two 10/100/1000 MBps Ethernet Ports • Two RS-232 Serial Ports • Front and Rear I/O • Integrated 1 MB L2 Cache • VxWorks BSP • Linux LSP
XPedite5000	Dual Gigabit Ethernet PMC (PrPMC)/XMC Module Based on the Motorola MPC8540 PowerQUICC III e50 • MPC8540 Up To 1GHz • Two 10/100/1000 MBps Gigabit Ethernet Interfaces • Front Or Rear I/O • 133 MHz/64-bit PCI-X • 500 MHz 8-bit RapidIO • Up to 1 GB SO-DIMM 333 MHz DDR SDRAM • 256 KB L2 Cache • Integrated Floating Point • 3-32 MB Soldered Flash • 2 UARTs • VxWorks Driver and BSP • Linux LSP XPedite5000 is an intelligent communications controller targeting high performance yet low cost applications • Powered by the MPC8540 (PowerQUICC IIITM), XPedite5000 supports two 10/100/1000 MBps Gigabit Ethernet, IEEE 802.3 compliant interfaces
XPort1001	A intelligent or non-intelligent, multi-protocol, four-port serial PMC (PrPMC) module • MPC8250 at up to 300 MHz with integrated PCI • Optional core-disable mode for operation as a low-cost, non-intelligent solution • Four SCCs support a broad range of serial protocols • Software-configurable serial interface modes • Front or rear I/O • 8 to 256 MB of SDRAM • 4 to 16 MB soldered Flash • 512 KB of socketed Flash • 2 KB EEPROM • Two RS-232 SMC ports • Optional back panel 10/100Base-T Ethernet • VxWorks driver and board support package • MontaVista Linux LSP
XPort3100	A dual Gigabit Ethernet PMC (PrPMC)/XMC module • MPC8540 processor at up to 1 GHz • Two 10/100/1000Base-T Ethernet interfaces • Front or rear I/O • 133 MHz/64-bit PCI-X • 500 MHz, 8-bit RapidIO • Up to 1 GByte SO-DIMM 333 MHz DDR SDRAM • 256 KB L2 cache • Integrated floating point • 4 to 96 MB soldered Flash • Two UARTs • VxWorks driver and board-support package • MontaVista Linux LSP
GE Fanuc Automation www.gefanuc.com/embedded	
PMC702	An intelligent processor PMC module • IBM PPC750FX processor at 800 MHz to 1.1 GHz • PCI and PCI-X interfaces • Master or peripheral PCI bus interface • 128, 256, or 512 MB of DDR memory • Single VxWorks
Interface Concept www.interfaceconcept.com	
IC-e6-PMCa	A low-power e600 PowerPC-based PrPMC • Designed around the Freescale MPC7447A, with support for the Freescale PowerPC product roadmap • Speed options up to 1.5 GHz • Up to 512 MB of DDR333 ECC SDRAM • 64 MB Flash EPROM • Optional SODIMM socket allows expandable SDRAM capability • Marvell Discovery III chipset • Three Gigabit Ethernet channels • Two multipurpose serial controllers • Backup SRAM • Real-time clock • Temperature sensor • JTAG/COP interface for probe debugging • Conformal coated and extended temperature versions available • Supports VxWorks and Linux
IC-PQ2-PMCa	A PrPMC (PMC processor) module • 300 MHz PowerQUICCII MPC8250 processor • Up to 128 MB of SDRAM • 8 MB of Flash memory • 128 KB of SRAM • Three 10/100Base-Tx ports on the front panel • One expansion slot for a PMC board on a Pn3 connector • Software support for VxWorks and Linux

Company name Model number	Description/Website
Kane Computing www.kanecomputing.com	
Zest100	A high-performance, FPGA processing engine • Single-sized Processor PMC module • Available with the Xilinx Virtex-II FPGA from 2V4000 to 2V8000 • Four I/O ports • 64-bit PCI controller and memory interfaces • Two bulk memory banks, one with 128 MB of SDRAM and one with 32 MB of DDR SDRAM • 16 MB of scratchpad memory in four DDR SRAM memory banks • 16 MB Flash memory • Four programmable clocks, external to the FPGA • Supports Windows 2000/XP, Linux, and VxWorks
Momentum Computer www.momenco.com	
Cheetah-Pr	An SBC in a 1.5-wide PMC form factor • Intel Pentium-M processor running at 1.1 GHz with a 400 MHz system bus frequency • 32-bit/33 MHz PCI bus Monarch PrPMC operation • Onboard PrPMC PCI bus arbitration on P4 connector • Up to 1 GByte of 64-bit DDR266 SDRAM with ECC • 1 MB firmware hub • SuperCap-backed real-time clock • Serial ATA interfaces on the PMC P4 connector Two USB ports on the front panel • Two 10/100/1000Base-T Ethernet links on the PMC P4 connector • One serial port on the PMC P4 connector • Gigabit Ethernet link/activity/speed LED indicator • Four user-defined LEDs through I/O controller hub GPIO signals • Supports Windows 2000/XP and Linux • Maximum power consumption of 25W
Cheetah-Prs	A single-wide PMC single board computer • Intel 855GME chipset, supports an Intel Pentium M processor • Intel 6300ESB I/O Controller Hub (ICH) • 400 MHz system bus • 10/100/1000Base-T Ethernet • PICMG compliant • Serial ATA interface • USB connectors • Front-panel HD-15 VGA interface • 1 MB firmware hub • Battery-backed real-time clock
Motorola www.motorola.com/computers	
PowerPMC-275	A PrPMC module based on the IBM PowerPC 750GX processor • Single or dual PowerPC 750GX processors at 1 GHz • Marvell Discovery II MV64360 system controller • Up to 1 GB of DDR SDRAM • Dual/independent Gigabit Ethernet interfaces • 1 MB boot Flash memory and 64 MB of user Flash • 64-bit/66 MHz PCI control plane • Dual serial interfaces • Multiple I2C EEPROM for board information and module configuration • 2 MB of integrated SRAM • Supports MontaVista Linux operating system • Single-image VxWorks BSP with loosely-coupled multiprocessing support
PrPMC880	A PowerPC-based PrPMC processor module • 1 GHz MPC7447 microprocessor with 128-bit Altivec technology • Up to 1 GByte of onboard DDR SDRAM • 72-bit ECC memory controller • 64 MB of Flash • Single-wide bridge • Async serial debug port • Four 32-bit timers • Two watchdog timers • Real-time clock • Optional front-panel or rear Pn4 I/O
N.A.T. www.nateurope.com	
NPMC-BRI	A standard CPU PMC mezzanine with four ISDN BRI (S0) interfaces • PowerQUICC processor at 33 MHz (40 or 50 MHz available) • SC4000 SCbus Controller • 4 or 16 MB of DRAM • Up to 4 MB of Flash • PCI bus controller • Operating system support includes VxWorks and pSOS+
Pentek www.pentek.com	
7110	A processor PMC card for digital signal processing • TMS320C44 processor provides 50 MFLOPS of processing power • 120 MBps data transfer rate over PCI bus • Four 20 MBps front-panel comm ports • 512 KB of zero wait state SRAM for global and local bus • Dual FIFO PCI interace using PLX 9080 • SwiftNet driver for 'C44 code development • Example software for host CPU boards
Prodrive www.prodrive.nl	
P3G4508	A low-cost G4 PowerPC PMC processor module • Motorola MPC741 processor at up to 500 MHz with MPX processor bus up to 133 MHz • Up to 2 MB of L2 cache • Up to 256 MB of SDRAM • Up to 32 MB of Flash • 32/64-bit 33/66 MHz PCI 2.2 interface • Three full-duplex 10/100Base-T Ethernet interfaces • Two full-duplex RS-232 serial interfaces • JTAG interface • Supports Linux and VxWorks
P4M480	A high-performance signal processing engine on a pipelined processor PMC module • Two TI C64x DSPs at 600 MHz • Xilinx Virtex-II XC2V8000 FPGA with 8 million system gates, DSP-to-DSP communication, and DSP-to-1394 communication • Up to 256 MB of SDRAM • 16 MB of Flash • 32-bit/33 MHz PCI 2.1 interface • Dual-port, 400 MBps IEEE-1394 interface • JTAG interface
RadiSys Corp www.radisys.com	
EPC-6321	933 MHz Intel Pentium III based PrPMC • 1 GB and 512 MB Memory Options • Dual Gigabit Ethernet • PICMG 2.15 Compatibility on EPC6321 • 74mm x 149mm streamlined PrPMC form factor • One Channel IDE • COM, Keyboard • System Monitoring, Watchdog Timer • Safety and EMC Compliance • VxWorks support
RT Logic! www.rtllogic.com	
RTL-DBP	A digital baseband processor in PMC form factor • Supports multiple baseband telemetry processing functions • PSK subcarrier demodulation: AGC with 60 dB gain for low-power signals, digital shaping filters, and demodulated baseband output • Bit synchronization with rates from 100 to 8 MBps, NRZ and Bi-phase PCM codes, and Viterbi decoder • Other application personalities: Frame synchronization up to 10 MBps, FSK demodulation, FM discriminator (IRIG formats), and SGLS FSK/AM command demodulation • Test code and device drivers • Full product documentation and customer support
RTL-DFP	A digital front-end processor in PMC form factor • Provides a modular, programmable platform for high-performance digital processing functions • Telemetry application personalities: Frame synchronizer/CCSDS transfer frame processor, Viterbi decoder, Reed Solomon Encoder/Decoder, PCM simulator/bit error rate tester, and IRIG time code processor (IRIGA, -B, -E, and -G) • Commanding application personalities: Format conversion (binary, ternary, Di-Bit), encryptor interface, echo checking, fill command/GCC generation, and CCSDS telecommand formatting/COP-1 processing
SBS Technologies www.sbs.com	
Palomar 1000 SFX or DFX	A single or dual PowerPC 750FX (667 MHz core/133 MHz 60x bus) processor PMC module • Up to 512 MB of SDRAM with ECC • Marvell GT64260 PCI bridge (32-bit/64-bit, 33 MHz/66 MHz) • 16 MB of soldered flash and 256 MB of IDE Flash • DFX version has two PowerPC 750FX processors at up to 1 GHz each
Sundance www.sundance.com	
SMT406	A Tangor FPGA-based processor PMC module • Tangor processing engine uses a Xilinx Virtex-II from 2V4000 to 2V10000 FPGA as the processing component • 128 MB of 133 MHz SDRAM, controlled by the PCI controller and accessible from both the PCI bus and the FPGA • Four banks of 4 MB each 200 MHz DDR SDRAM connected to the FPGA • One bank of 32 MB 250 MHz DDR SDRAM connected to the FPGA • 16 MB of Flash available for configuration and user-defined purposes • All memory banks have 64-bit data paths (Flash is 8 bits) • Two programmable clocks generate up to 500 MHz and two others generate up to 120 MHz • JTAG header • Four I/O ports: PCI via PCI controller, PMC user-defined I/O, 60-pin Micror header, and front-panel I/O
Technobox www.technobox.com	
3797	A x86 platform on PMC for embedded applications • Single-wide • National Semiconductor SC2200 GEODE processor includes video, DRAM control, interfaces for PCI bus and IDE devices • 300 MHz, with 100 MHz SDRAM bus speed • 128 MB SDRAM • 6W total power consumption • Can be configured as either a co-processor or a PrPMC system host • Operational mode is managed by an Altera 1K100 PLA that controls the interface between the GEODE PCI local bus and the PMC PCI bus, depending on code downloaded from Flash memory at startup • Supports front panel connection of peripherals through an external, cable-attached breakout board • Supports USB and standard COM ports as well as DVI and SVGA video 10/100Base-Tx Ethernet • 16-bit wide IDE interface at the Pn4 connector to allow attachment of a CD-ROM or other IDE component • Supports Windows 98/2000 and Linux within embedded applications
Zephyr Engineering www.zpci.com	
PrPMC800 Mon-arch CPU	A PMC CPU module • 450 MHz Motorola MPC7410 CPU • 128 MB of PC100 ECC SDRAM memory • 32 MB of FLASH memory • RS-232 port • Bank B Flash port • JTAG debug port

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By Chad Lumsden

BACKPLANE: SWITCHED FABRIC

APW

Website: www.apw.com

Model: cPCI EtherPlane Backplane **RSC No:** 19712
Up to 21 slots in a 19" rack or more for 23" racks (up to 24 node slots) • Compliance to PICMG 2.16 • Compliance to PICMG 2.0 rev. 3.0 • Supports PICMG 2.1 rev. 2 for basic hot swap • 64 bit PCI bus • Optional configurations for System Slot as a Node Slot • Configurations available with H.110 bus (PICMG 2.5) with provisions for Telecoms Power • Configurations available with dual hot swappable power supplies • 6U form factor • Supports PICMG 2.9 System Management • 15 slots has provisions for 1 bridge, or a 21 slot with 2 bridges • With a 21 slot backplane, 1 segment can be run at 66 MHz • Other slot sizes and configurations are available upon request

CHIPS & CORES: SOC

MIPS Technologies

Website: www.mips.com

Model: SOC-it OCP Controller **RSC No:** 19822
An OCP system controller optimized for the MIPS32 24K core family • Tightly coupled memory controller and multiple, high bandwidth, dual-port interfaces to Intellectual Property (IP) blocks • Point-to-point switched bus interconnects • Supports vectored interrupts with software examples for interrupt handlers • Memory arbiter can be modified to prioritize data packets • Full compliance to industry standard buses • Fully static design enables low power operation

RF Microdevices

Website: www.rfmd.com

Model: SiW4000 **RSC No:** 19821
A System-on-Chip Bluetooth solution with Enhanced Data Rate (EDR) • Specifically designed for mobile phone applications • 0.13 micron CMOS process for low current consumption, small size, and low cost • Direct connection to the battery for efficient power management • Direct conversion architecture for superior performance, including low spurious emissions and enhanced RF blocking • On-chip 50 ohm matching network • High-speed synchronous and asynchronous serial interface capable of supporting EDR data rates • Direct input from mobile phone reference clocks • Industry-standard ARM7 TDMI processor core • Stacked Flash package footprint compatible with the ROM package



RSC #19821

COMPONENT-LEVEL MODULES

Linear Technology

Website: www.linear-tech.com

Model: LTC4221 **RSC No:** 19820
A dual hot-swap controller with a dual-level circuit breaker • Allows safe board insertion and removal from a live backplane • Configurable power supply sequencing • Soft start with current foldback limits inrush current • No external gate capacitor required • Adjustable dual-level circuit breaker protection • Controls supply voltages from 1 V to 13.5 V • Independent N-channel FET high-side drivers • FB pins monitor Vout for overvoltage protection • Latch off or automatic retry on current fault • FAULT and PWRGD outputs • Narrow 16-pin SSOP package

DATACOM: SERIAL CONTROLLER

Concurrent Technologies

Website: www.gocct.com

Model: cc PMC/232 **RSC No:** 19817
A PMC mezzanine multi-serial communication and parallel printer interface • Two National Semiconductor Super I/O controllers • Four communication channels with 115 Kbaud asynchronous data rates • Single parallel interface (EPP, ECP, and IEEE 1284 compatible) • 64 KB FLASH EPROM • Software support includes UnixWare, Windows NT, VxWorks, QNX, and Solaris

DATACOM: WAN

Performance Technologies

Website: www.pt.com

Model: PCI334A **RSC No:** 19753
Multipurpose intelligent WAN communications adapter • Four high-speed channels capable of sustaining 2 MBps per port • Four MB of shared SRAM memory • Universal I/O supporting 3.3V and 5V • Support for 33 MHz and 66 MHz PCI Bus • Increased RS-232 support allowing for data transmission range of up to 100 Kbps • Existing PCI334 software compatible with PCI334A • Integrated WAN Communications Software includes Radar Receiver/SBSI, HDLC, Frame Relay, LAPD and X.25 • Broad operating system support includes: Solaris, Windows NT, and Linux

DSP RESOURCE BOARDS: PMC

Evergreen Group

Website: www.evergreengrp.com

Model: VT-1423 **RSC No:** 19813
DSP PMC modules based on the TI TMS320C6415 or TMS320C6416 processors • Available in a dual processor format • Clock speeds of up to 720 MHz • 0, 16, 32, or 64 MB of SDRAM • 0, 1, or 2 MB of Flash • Utopia Level II interface on P14 • Single-width IEEE 1386.1 PMC module • Code development and debug using an emulator via JTAG header • 64-bit/66 MHz universal PCI interface • Complete set of code development tools available for Windows

FABRICS: FIBRE CHANNEL

Astek Corporation

Website: www.astekcorp.com

Model: A7202CP **RSC No:** 19690
Two independent, 2 Gb Fibre Channels (up to

400 MBps, full duplex) • Rear I/O Capability • SFP, supports multi-mode optics and copper options • 64-bit, 33/66 MHz PMC • Bridgeless, full hot swap capability • Auto-negotiation for legacy connect (1 or 2 Gb) • Concurrent SCSI and IP protocol • Software supports switch and loop (private and public) topologies • FC-Tape Support • SNIA HBA API compliant • MPT Flash utility • Remote updates of firmware and FCODE • FusionMPT TM architected • SANmark TM approved • Supports all major OSs • 3 year limited warranty

Astek Corporation

Website: www.astekcorp.com

Model: A7202Z **RSC No:** 19689
Two independent, 2 Gb Fibre Channels • Rear I/O Capability • SFP, supports multi-mode optics and copper options • 64-bit, 33/66 MHz PMC • Auto-negotiation for legacy connect (1 or 2Gbit) • MPT Flash utility-remote updates of firmware and FCODE • Concurrent SCSI and IP protocol • FC-Tape Support • Software supports switch and loop (private and public) topologies • SNIA HBA API compliant • CIM based server management • Supports all major OSs • Fusion-MPT TM architected • 3 year limited warranty

GATEWAYS

Pinnacle Data Systems

Website: www.pinnacle.com

Model: TS2100 **RSC No:** 19685
Layer 4 - 7 packet classification • Linux 2.4.2 Kernel optimized for PowerPC • Enhanced Protocol Stack (contact ZNYX for details) • FTP, TFTP, Telnet - (Server/Client) • DHCP Server/Client/Relay • Network File Server / Web Server • Network Address Translation (RFC1631) • 802.1Q VLAN with GARP, GMRP, GVRP • 802.1D Spanning Tree with 802.1w • Rapid Spanning Tree Algorithm (RSTP) • Virtual Router Redundancy Protocol (RFC2338) • IP Multicast Support • IGMP Snooping, IGMPv1, IGMPv2, DVMRP • IEEE802.1p Traffic Class/Priority Queues • Differentiated Services for QoS • SNMPv1, SNMPv2, SNMPv3 • MIB-II (RFC1213) (RFC2013) • VLAN Extension MIB (RFC2674) • 802.1D Spanning Tree MIB • RMON and RMONv2 MIB • Commercial Open Policy Service (COPS) • COPS-PR (Provisioning) Sun



RSC #19685

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